CoreModule® 720
Single Board Computer
Reference Manual

P/N 50-1Z105-1000

Notice Page

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REVISION HISTORY

Revision	Reason for Change	Date
1000	Initial Release	Jan/12

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

Contents

Chapter 1 About This Manual 1
Purpose of this Manual 1
References 1
Chapter 2 Product Overview 3
PC/104 Architecture 3
Product Description 4
Module Features 5
Block Diagram 7
Major Component (ICs) Definitions 8
Header, Connector, and Socket Definitions 11
Jumper Header Definitions 13
Specifications 14
Physical Specifications 14
Mechanical Specifications 15
Power Specifications 16
Environmental Specifications 16
Thermal/Cooling Requirements 17
Chapter 3 Hardware 19
Overview 19
CPU 20
Graphics 20
Memory 20
Interrupt Channel Assignments 21
Memory Map 21
I/O Address Map 22
Serial Interfaces 23
USB Interfaces 24
Ethernet Interface 26
Video (SDVO/LVDS) Interfaces 27
Power Interface 29
User GPIO Interface 29
Utility Interface 30
Power Button 30
Reset Switch 30
Speaker 30
System Management Bus (SMBus) 31
CAN Bus Interface 31
I2C Interface 32
System Fan 32
Battery 32
Ethernet External LED 33
Miscellaneous 33
SSD (Solid State Drive) 33
Real Time Clock (RTC) 33
Oops! Jumper (BIOS Recovery) 33

Serial Console 34
Serial Console Setup 34
Hot (Serial) Cable 34
Watchdog Timer 34
Chapter 4 BIOS Setup 35
Introduction 35
Entering BIOS Setup (Local Video Display) 35
Entering BIOS Setup (Serial Port Console) 35
OEM Logo Utility 36
Logo Image Requirements 36
BIOS Setup Menus 37
Main BIOS Setup Screen 37
Advanced BIOS Setup Screen 38
Chipset BIOS Setup Screen 41
Boot BIOS Setup Screen 43
Security BIOS Setup Screen 44
Save & Exit BIOS Setup Screen 45
Appendix A Technical Support 47
Index 49

List of Figures

Figure 2-1. Stacking PC/104-Plus Modules with the CoreModule 720 4
Figure 2-2. Functional Block Diagram 7
Figure 2-3. Component Locations (Top Side) 10
Figure 2-4. Component Locations (Bottom Side) 10
Figure 2-5. Connector Pin Sequences 12
Figure 2-6. Header, Connector, and Socket Locations (Top Side) 12
Figure 2-7. Jumper Header Locations (Top Side) 13
Figure 2-8. Mechanical Overview (Top Side) 15
Figure 2-9. Stack Height of Cooling Assembly 17
Figure 3-1. Oops! Jumper Serial Port (DB9) 33
Figure 3-2. Serial Console Jumper 34
Figure 4-1. Main BIOS Setup Screen 37
Figure 4-2. Advanced BIOS Setup Screen 38
Figure 4-3. Chipset BIOS Setup Screen 41
Figure 4-4. Boot BIOS Setup Screen 43
Figure 4-5. Security BIOS Setup Screen 44
Figure 4-6. Save & Exit BIOS Setup Screen 45

List of Tables

Table 2-1. Major Component Descriptions and Functions 8
Table 2-2. Module Header and Connector Descriptions 11
Table 2-3. Jumper Settings 13
Table 2-4. Weight and Footprint Dimensions 14
Table 2-5. Power Supply Requirements 16
Table 2-6. Environmental Requirements 16
Table 3-1. Interrupt Channel Assignments 21
Table 3-2. Memory Map 21
Table 3-3. I/O Address Map 22

Table 3-4. Serial 1 (COM0) Interface Pin Signal Descriptions (J10) 23
Table 3-5. Serial 2 (COM1, 2, and 3) Interface Pin Signal Descriptions (J11) 24
Table 3-6. USB0 and USB1 Interface Pin Signals (J12) 24
Table 3-7. USB2 and USB3 Interface Pin Signals (J14) 25
Table 3-8. USB4 and USB5 Interface Pin Signals (J13) 25
Table 3-9. Ethernet Interface Pin Signal Descriptions (J8) 26
Table 3-10. SDVO Interface Pin Signals (J15) 27
Table 3-11. LVDS Video Interface Pin Signals (J23) 28
Table 3-12. Power Interface Pin Signals (J19) 29
Table 3-13. User GPIO Interface Pin Signals (J3) 29
Table 3-14. Utility Interface Pin Signals (J22) 30
Table 3-15. SMBus Reserved Addresses 31
Table 3-16. SMBus Pin Signals (J24) 31
Table 3-17. CAN Interface Pin Signals (J4) 31
Table 3-18. I2C Interface Pin Signals (J6) 32
Table 3-19. System Fan Pin Signals (J21) 32
Table 3-20. External Battery Input Header (J20) 32
Table 3-21. Ethernet External LED Pin Signals (J9) 33
Table 4-1. BIOS Setup Menus 37
Table A-1. Technical Support Contact Information 47

Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the CoreModule® 720 Single Board Computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- Product Overview
- Hardware Specifications
- BIOS Setup information
- Technical Support Contact Information

Information not provided in this reference manual includes:

- Detailed chip specifications (refer to the References section of this chapter)
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry-standard busses and signals
- Pin-signal definitions for industry-standard interfaces

References

The following list of references may help you successfully complete your custom design.

Expansion Bus Specifications

- PC/104 Specification, Revision 2.5, November, 2003
- PC/104-Plus Specification, Revision 2.0, November, 2003

  Web site: http://www.pc104.org
- PCI Specification, Revision 3.0, August 12, 2002

  Web site: http://www.pcisig.com
- LPC Bus Specification, Revision 1.1, August, 2002

  Specification: http://www.intel.com/design/chipsets/industry/25128901.pdf
- PCIe Specification, Revision 1.0a, April 15, 2003

  Specification (for members): http://www.pcisig.com/specifications/pciexpress/base/archive/
- I^2C Bus Specification Version 2.1

  Specification: http://www.nxp.com/documents/other/39340011.pdf
- AMI BIOS Aptio TSE User's Guide

  Data sheet: http://www.ami.com/support/doc/AMI_TSE_User_Manual_PUB.pdf
- Bosch CAN specification version 2.0B

  Specification: http://www.can-cia.org/fileadmin/cia/specifications/CAN20B.pdf

Chip Specifications

The following integrated circuits (ICs) are used in the CoreModule 720 single board computer:

- Intel® Corporation and the Atom™ E6XXT processors

  Data sheet: http://download.intel.com/embedded/processor/datasheet/324208.pdf

- Hynix Semiconductor, Inc. and the H5PS2G83AFR-S6C DDR2 on-board System Memory

  Web site: http://www.hynix.com/gl/products/computing/computing_info.jsp

- Intel Corporation and the PCH EG20T chip, used for the I/O Hub (Southbridge)

  Data sheet: http://download.intel.com/embedded/chipsets/datasheet/324211.pdf

- Texas Instruments and the SN65HVD1040D CAN Transceiver

  Web site: http://focus.ti.com/lit/ds/symlink/sn65hvd1040.pdf

- Intel Corporation and the 82574IT chip used for the Gigabit Ethernet controller

  Data sheet: http://download.intel.com/design/network/datashts/82574.pdf

- Atmel Corporation and the AT25128B-SSHL-B Ethernet EEPROM

  Data sheet: http://www.atmel.com/dyn/resources/prod_documents/doc8535.pdf

- Fintek and the F85226FG, LPC-to-ISA Bridge

  Data sheet:

  http://pdf1.alldatasheet.com/datasheet-pdf/view/257962/FINTEK/F85226FG.html

- PLX Technology and the PEX8112 PCIe-to-PCI Bridge

  Data sheet:

  http://www.plxtech.com/products/expresslane/pex8112#technicaldocumentation

- Atmel Corporation and the AT25640B-SSHL SPI EEPROM

  Data sheet: http://www.atmel.com/dyn/resources/prod_documents/doc8535.pdf

- Maxim Integrated Products and the MAX3245EEUI+ RS-232 Serial Port Transceiver

  Web site: http://www.maxim-ic.com/datasheet/index.mvp/id/1847

- Analog Devices and the ADM1032ARMZ Temperature Monitor

  Data sheet: http://www.onsemi.com/pub_link/Collateral/ADM1032-D.PDF

- Greenliant and the GLS85LS1008A Solid State NANdrive

  Data sheet: http://www.greenliant.com/dotAsset/45628.pdf

NOTE	If you are unable to locate the datasheets using the links provided, search the internet using the name of the manufacturer or component model and locate the documents you need.

Chapter 2 Product Overview

This overview presents general information about the PC/104 architecture and the CoreModule 720 Single Board Computer (SBC). After reading this chapter you should understand:

- PC/104 architecture
- Product description
- Major components (ICs)
- Headers, Connectors, and Sockets
- Specifications

PC/104 Architecture

The PC/104 architecture affords a great deal of flexibility in system design. You can build a simple system using only a CoreModule 720 SBC, input/output devices connected to the serial, USB, or SATA ports, and the on-board Solid State Disk storage device. To expand a simple CoreModule system, simply add self-stacking PC/104 and PC/104-Plus expansion boards to provide additional capabilities, such as:

- Additional serial and parallel ports
- Analog or high-speed digital I/O
    - Data Acquisition (Analog In/Out)
    - USB 2.0 expansion modules
    - IEEE 1394 (FireWire) expansion modules
    - Standard VGA video output

PC/104 or PC/104-Plus expansion modules can be stacked with the CoreModule 720 avoiding the need for large, expensive card cages and backplanes. The PC/104-Plus expansion modules can be mounted directly to the PC/104 and PC/104-Plus connectors of the CoreModule 720. PC/104-compliant modules can be stacked with an inter-board spacing of ~0.6 inches, so that a 3-module system fits in a 4.6" x 3.8" x 2.0" space. See Figure 2-1.

One or more MiniModule products or other PC/104 modules can be installed on the CoreModule expansion connectors, so that the expansion modules fit within the CoreModule outline dimensions. Most MiniModule products have stackthrough connectors compatible with the PC/104-Plus Version 2.0 specification. Several modules can be stacked on the CoreModule headers. Each additional module increases the thickness of the package by ~17mm (0.6"). See Figure 2-1.

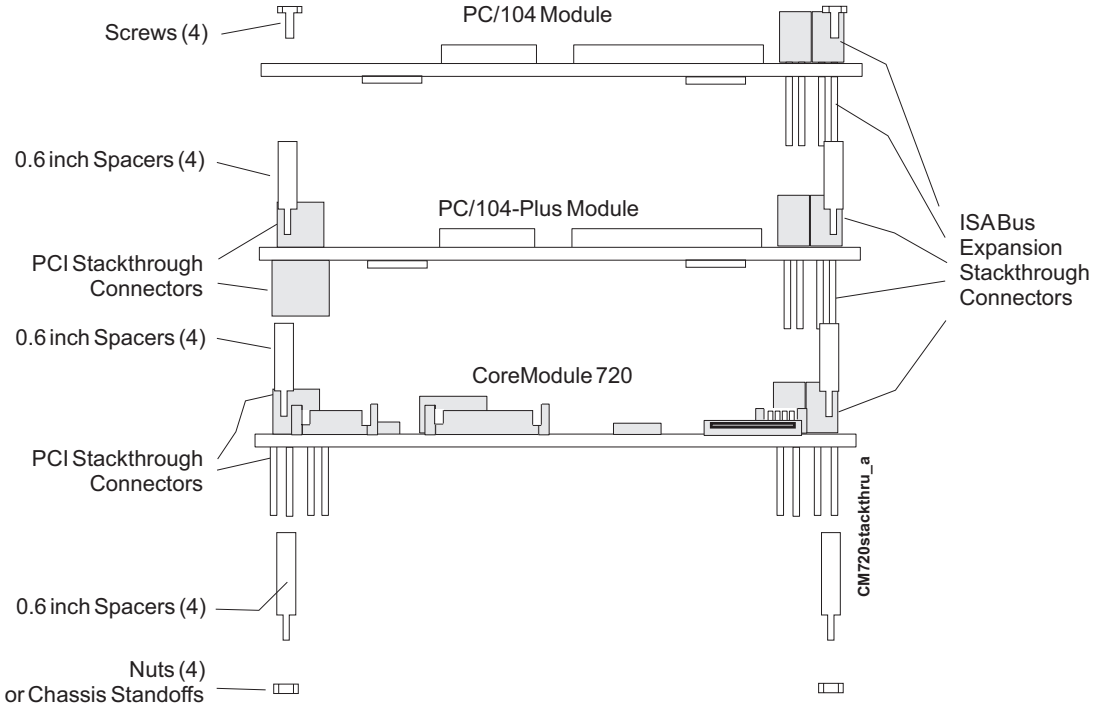

Figure 2-1. Stacking PC/104-Plus Modules with the CoreModule 720

Product Description

The CoreModule 720 SBC is a highly integrated, high performance, Intel® Atom™ E6XXT processor based system, compatible with the PC/104 standard. This rugged and high quality single-board system contains all the component subsystems of an ATX motherboard, plus the equivalent of several PCI expansion boards.

The Intel Atom E6XXT series CPUs integrate processor cores with Graphics and Memory Controller Hubs (GMCHs), providing low-power, high-performance processors, memory controllers for up to 2GB of DDR2 on-board memory, and graphics controllers which provide LVDS and SDVO signals for most LCD video panels and CRT monitors.

The EG20T PCH (Platform Controller Hub) provides the I/O hub for a range of common interfaces including six USB ports, four serial ports, and two SATA ports, as well as embedded interfaces for CAN, GPIO, I2C, and SDIO. The CoreModule 720 provides a Solid State Drive through the SATA1 port and an SD memory card socket through the SDIO port. The PCH connects to the CPU through the PCIe Port0, and a Gigabit Ethernet controller connects to the CPU through PCIe Port2.

The CoreModule 720 can be expanded through the LPC and PCIe expansion buses using the PC/104 and PC/104-Plus connectors for additional system functions. These buses offer compact, self-stacking, modular expandability. The PC/104 bus is an embedded system version of the signal set provided on a desktop PC's ISA bus. The PC/104-Plus bus includes this signal set plus additional signals implementing a PCI bus, available on a 120-pin (4 rows of 30 pins) PCI expansion bus connector. This PCI bus operates at a clock speed of up to 66MHz, and the ISA bus operates at 8MHz.

The CoreModule 720 is particularly well suited to either embedded or portable applications and meets the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with ADLINK MiniModules™ or other PC/104-compliant expansion modules, or it can be used as a powerful computing engine. The CoreModule 720 requires a single +5V AT power source.

Module Features

- CPU
  - Provides a 600MHz, 1.3GHz, or 1.6GHz Intel Atom E620T, E660T, or E680T Processor Core and Graphics Memory Controller Hub
  - Provides Enhanced SpeedStep® technology
  - Supports Hyper-Threading Technology
  - Provides on-die 512-kB, 8-way L2 cache
  - Provides L2 Dynamic Cache Sizing
  - Supports 32-bit physical addresses and 48-bit linear addresses
  - Provides 3D graphics engine
  - Provides single-channel DDR2 memory controller
- Memory
  - Provides up to 2 GB of +1.8V DDR2 soldered, on-board memory
  - Provides double data rate interface
  - Supports 32-bit data bus
  - Supports DDR2 800MHz memory
  - Provides non-ECC, unbuffered memory
- Expansion Buses
  - PC/104 bus speeds up to 14MHz (16-bit ISA Bus)
  - PC/104-Plus bus speed at up to 66MHz (32-bit PCI Bus)
  - PCI 3.0 bus
  - I2C 2.1 bus
  - Bosch CAN protocol version 2.0B Active
- SATA Interface
  - Supports two SATA ports from the EG20T PCH (one used for SSD)
  - Provides one standard SATA connector
  - Supports on-board Solid State Drive (SSD) with default 8GB capacity
- Serial Interface
  - Provides four buffered serial ports (COM0-3), with full handshaking on the COM0 port
  - Provides 16550-equivalent controllers with 256-byte FIFO mode on the COM0 port and 64-byte FIFO mode on the COM1-3 ports
  - Supports full-duplex buffering and full status reporting
  - Supports full modem capability on COM0 port
  - Supports programmable baud-rate generator
    - COM0: 300bps to 4Mbps
    - COM1, 2, and 3: 300bps to 1Mbps
- CAN Interface
  - Supports bit rate up to 1 Mbps
  - Supports 32 message objects

- USB Interface
  - Provides three root USB hubs
  - Provides up to six USB ports
  - Supports USB boot devices
  - Supports USB Keyboard and Mouse
  - Supports USB v2.0 EHCI and v1.1 UHCI
  - Supports over-current detection status
- Ethernet Interface
  - Provides one fully independent Ethernet port
  - Provides integrated LEDs on each port (Link/Activity and Speed)
  - Provides one Intel 82574IT controller chip
  - Provides header for LAN LED signals (Gigabit only)
  - Supports IEEE 802.3 10/100BaseT and 10/100/1000BaseT compatible physical layers
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full duplex mode
    - Half-duplex mode supports enhanced proprietary collision reduction mode
- Video Interfaces (SDVO and LVDS)
  - Provide SDVO outputs
    - Resolutions up to 1280x1024 @ 85Hz
    - A variety of external display technologies such as DVI, TV-Out, and CRT
    - Maximum pixel clock rate up to 160MHz
  - Provide LVDS flat panel outputs
    - Resolutions up to 1280x768 @ 60Hz
    - Minimum pixel clock rate of 19.75MHz
    - Maximum pixel clock rate of 80MHz
    - Pixel color depths of 18 and 24 bits
- Utility Interface
  - Power Button
  - Reset Switch
  - Speaker
- Miscellaneous
  - Real Time Clock (RTC) with external replaceable battery
  - Battery-free boot
  - Oops! Jumper support
  - Serial Console support
  - Watchdog Timer
  - Logo Screen (Splash)

Block Diagram

Figure 2-2 shows the functional components of the CoreModule 720.

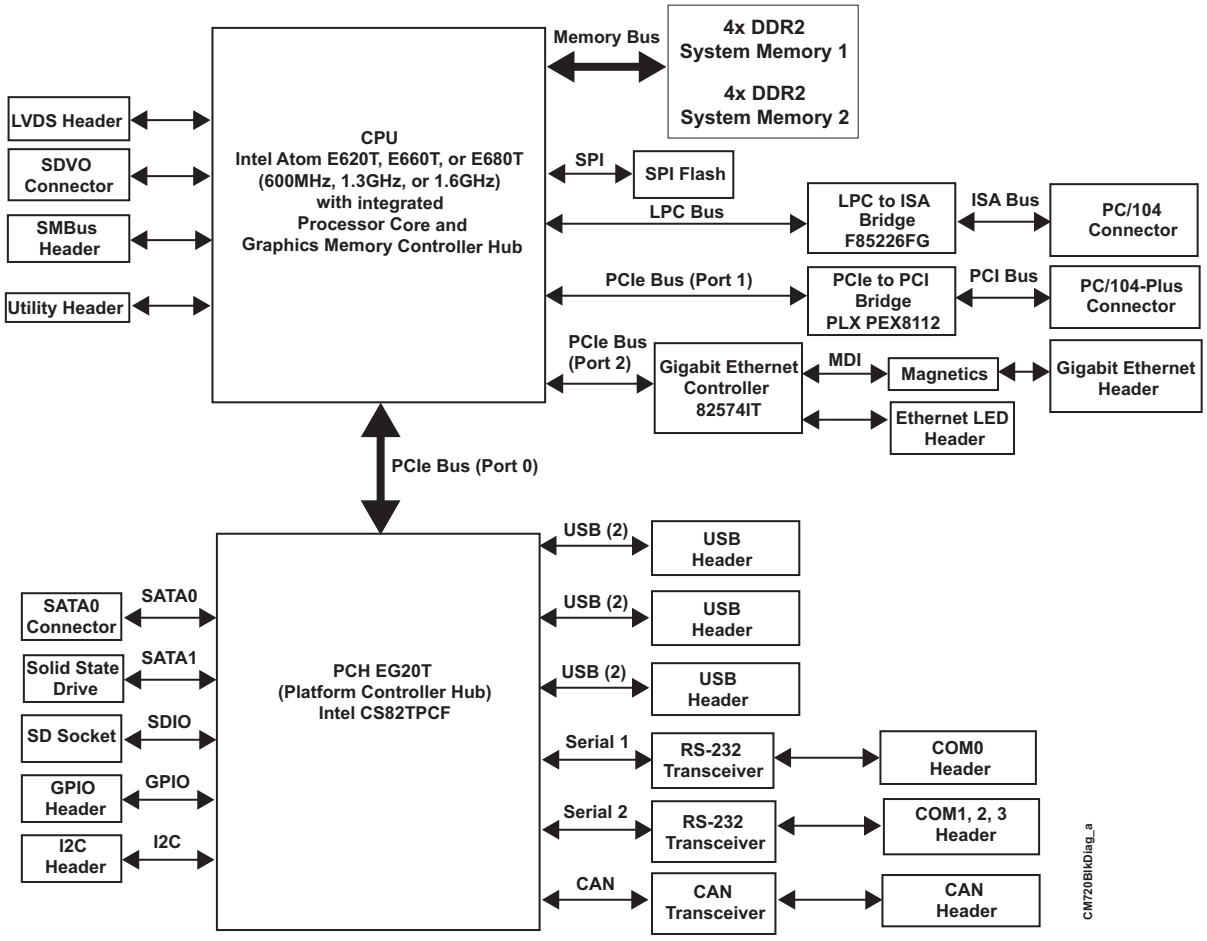

Figure 2-2. Functional Block Diagram

Major Component (ICs) Definitions

Table 2-1 lists the major ICs, including a brief description of each, on the CoreModule 720. Figures 2-3 and 2-4 show the locations of the major ICs.

Table 2-1. Major Component Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel	Atom E620T, E660T, or E680T	600MHz, 1.3GHz, or 1.6GHz processor with 8-way L2 cache	Integrates Processor Core and Graphics Memory Controller Hub
DDR2 Memory - 1 (U2, U3, U4, U5)	Hynix	H5PS2G83AFR-S6C	On-board DDR2 System Memory - 1	Provides high-speed data transfer
DDR2 Memory - 2 (U6, U7, U8, U9 - on bottom side [see Figure 2-4])	Hynix	H5PS2G83AFR-S6C	On-board DDR2 System Memory - 2	Provides high-speed data transfer
PCH [Platform Controller Hub (U10)]	Intel	CS82TPCF (PCH EG20T)	I/O Hub for common user interfaces	Provides Southbridge interfaces and off loads some Northbridge functions from the CPU
CAN Transceiver (U12 - on bottom side [see Figure 2-4])	Texas Instruments	SN65HVD1040D	Transceiver for Controller Area Network (CAN)	Provides up to 1 Mbps of differential transmit and receive capabilities for the CAN controller in the PCH
Gigabit Ethernet Controller (U15)	Intel	82574IT	Gigabit Ethernet controller	Generates PCIe 10T/100TX/ 1000T Ethernet signals
Ethernet EEPROM (U16)	Atmel	AT25128B-SSHL-B	Three-Wire Serial EEPROM for Gigabit Ethernet Controller	Provides storage for MAC addresses, serial numbers, and pre-boot configuration data
LPC-to-ISA Bridge (U17 - on bottom side [see Figure 2-4])	Fintek	F85226FG	LPC-to-ISA interface	Migrates legacy ISA interfaces
PCIe-to-PCI Bridge (U18)	PLX Technology	PEX8112	PCIe-to-PCI interface	Migrates legacy PCI interfaces

Table 2-1. Major Component Descriptions and Functions (Continued)

SPI EEPROM (U20 - on bottom side [see Figure 2-4])	Atmel	AT25640B-SSHL	Electronically-erasable programmable read-only memory	Stores PCIe-to-PCI bridge configuration data
RS-232 Transceiver (U21)	Maxim	MAX3245EEUI+	Transceiver for Serial 1 RS-232 signals	Transmits and receives RS-232 signals for COM0
RS-232 Transceiver (U22)	Maxim	MAX3245EEUI+	Transceiver for Serial 2 RS-232 signals	Transmits and receives RS-232 signals for COM1, 2, & 3
SPI Flash (U31)	SST	SST25VF016B-50-4C-52AF	Serial Peripheral Interface Flash Memory chip (for firmware)	Stores BIOS in Flash Memory
Thermal Regulator - PCIe-to-PCI Bridge (U32 - on bottom side [see Figure 2-4])	AME	AME8850AEEVADJZ	Linear Regulator	Provides power-saving mode, over-current protection, and thermal shutdown for the PCIe-to-PCI Bridge
Temperature Monitor (U33)	Analog Devices	ADM1032ARMZ	Digital thermometer for CPU temperature	Measures the temperature output of the CPU and provides over-temperature alarm
Thermal Regulator - SSD (U35)	AME	AME8850AEEVADJZ	Linear Regulator	Provides power-saving mode, over-current protection, and thermal shutdown for the Solid State Drive
Solid State Drive [SSD] - SATA (U37 - on bottom side [see Figure 2-4])	Greenliant	GLS85LS1008A	Industrial-grade, soldered solid state storage module	Provides solid state storage through the SATA interface
Transformer - Gigabit Ethernet (T1)	Wurth Elektronik	7490200110	Gigabit Ethernet Magnetics	Provides electrical isolation for Gigabit Ethernet controller

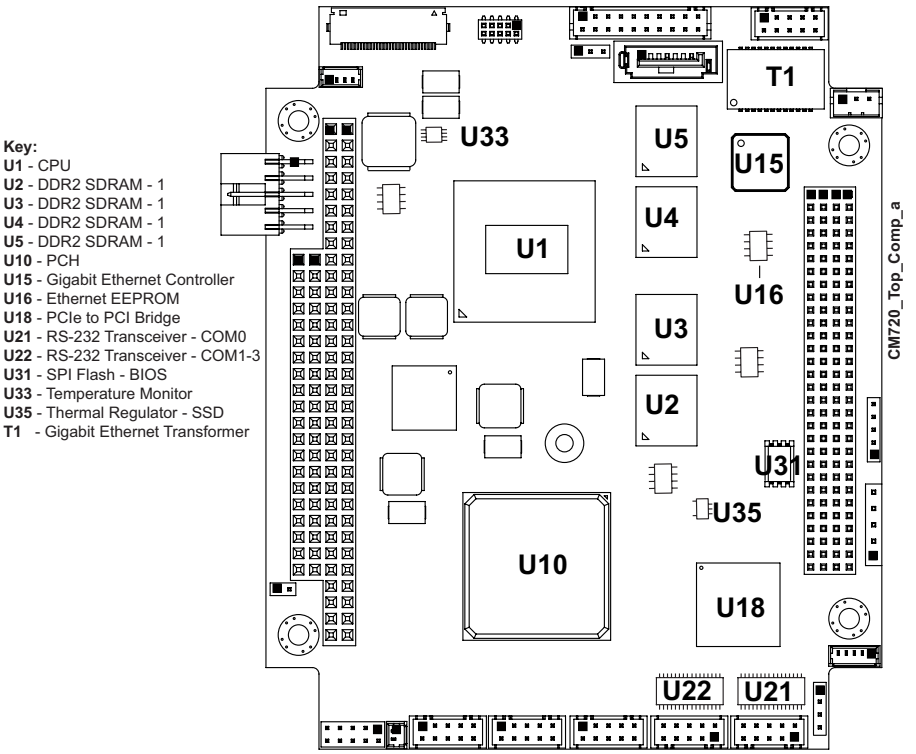

Figure 2-3. Component Locations (Top Side)

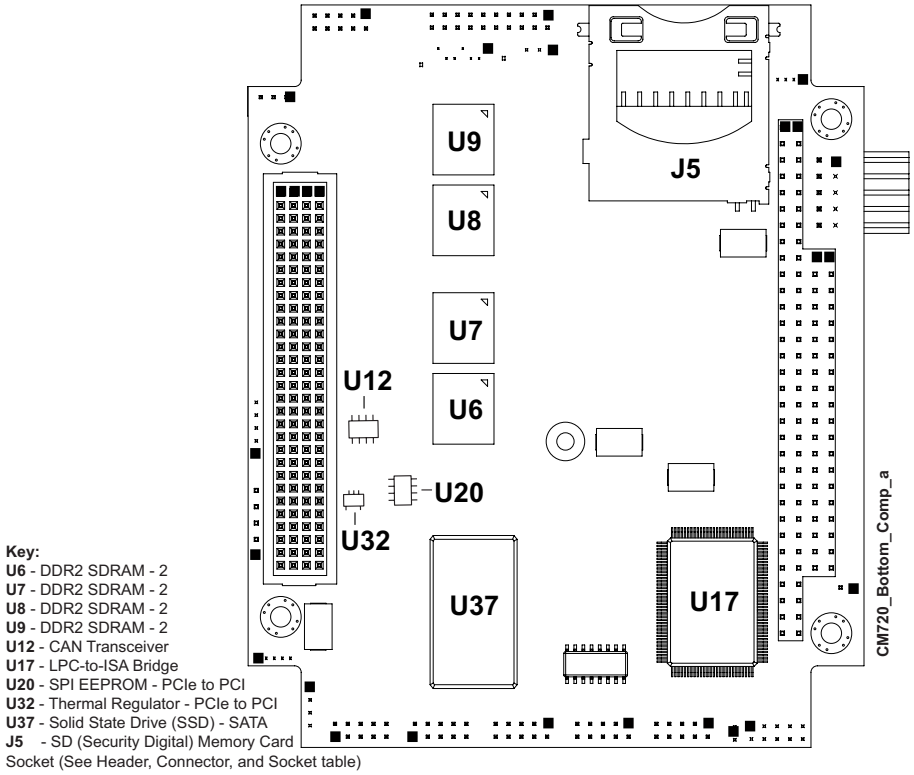

Figure 2-4. Component Locations (Bottom Side)

Header, Connector, and Socket Definitions

Table 2-2 describes the headers, connectors, and socket of the CoreModule 720 shown in Figure 2-6.

Table 2-2. Module Header and Connector Descriptions

Header #	Board Access	Description
J1 – LPC Debug	Top	10-pin, 0.050" (1.27mm) female debug port header for issues such as Port 80 POST errors
J3 – GPIO	Top	10-pin, 0.079" (2mm) header for General Purpose IO signals
J4 – CAN	Top	4-pin, 0.079" (2mm) header for transmitting and receiving Controller Area Network signals
J5 – SD Memory Socket	Bottom (See Figure 2-4)	9-pin standard socket for Security Digital Memory cards
J6 – I^2C	Top	5-pin, 0.079" (2mm) header for I^2C bus
J7 – SATA0	Top	7-pin, 0.050" (1.27mm) standard connector for SATA devices
J8 – Ethernet - Gigabit	Top	10-pin, 0.079" (2mm) shrouded header for Gigabit Ethernet port
J9 – LED Ethernet - Gigabit	Top	4-pin, 0.049" (1.25mm) shrouded header for Ethernet LED signals
J10 – Serial 1	Top	10-pin, 0.079" (2mm) shrouded header for the COM0 signals
J11 – Serial 2	Top	10-pin, 0.079" (2mm) shrouded header for the COM1, 2, and 3 signals
J12 – USB 0-1	Top	10-pin, 0.079" (2mm) shrouded header for USB0 and USB1 signals
J13 – USB 4-5	Top	10-pin, 0.079" (2mm) shrouded header for USB4 and USB5 signals
J14 – USB 2-3	Top	10-pin, 0.079" (2mm) shrouded header for USB2 and USB3 signals
J15 – SDVO	Top	30-pin, 0.020" (0.5mm) flip-lock, bottom-contact FPC connector for single-channel SDVO interface
J17 – PC/104-Plus	Top/Bottom	120-pin, 0.079" (2mm) standard connector for PC/104-Plus signals
J18 – PC/104	Top/Bottom	104-pin, 0.100" (2.54mm) standard connector for PC/104 signals
J19 – Power	Top	10-pin, 0.100" (2.54mm) right-angle, shrouded header for external power connection
J20 – Battery	Top	2-pin, 0.049" (1.25mm) shrouded header for power from external battery
J21 – Fan	Top	3-pin, 0.079" (2mm) shrouded header for System Fan signals
J22 – Utility	Top	5-pin, 0.100" (2.54mm) single-row header for Power Button, Reset Switch, and Speaker signals
J23 – LVDS	Top	20-pin, 0.079" (2mm) shrouded header for LVDS video signals
J24 – SMBus	Top	5-pin, 0.079" (2mm) single-row header for SMBus signals

NOTE The pinout tables in Chapter 3 of this manual identify pin sequence using the following method: A 10-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as 10-pin, 2 rows, odd/even (1, 2). See Figure 2-5.

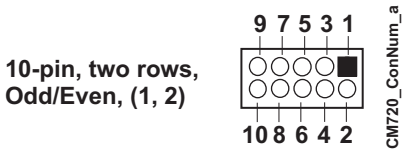

Figure 2-5. Connector Pin Sequences

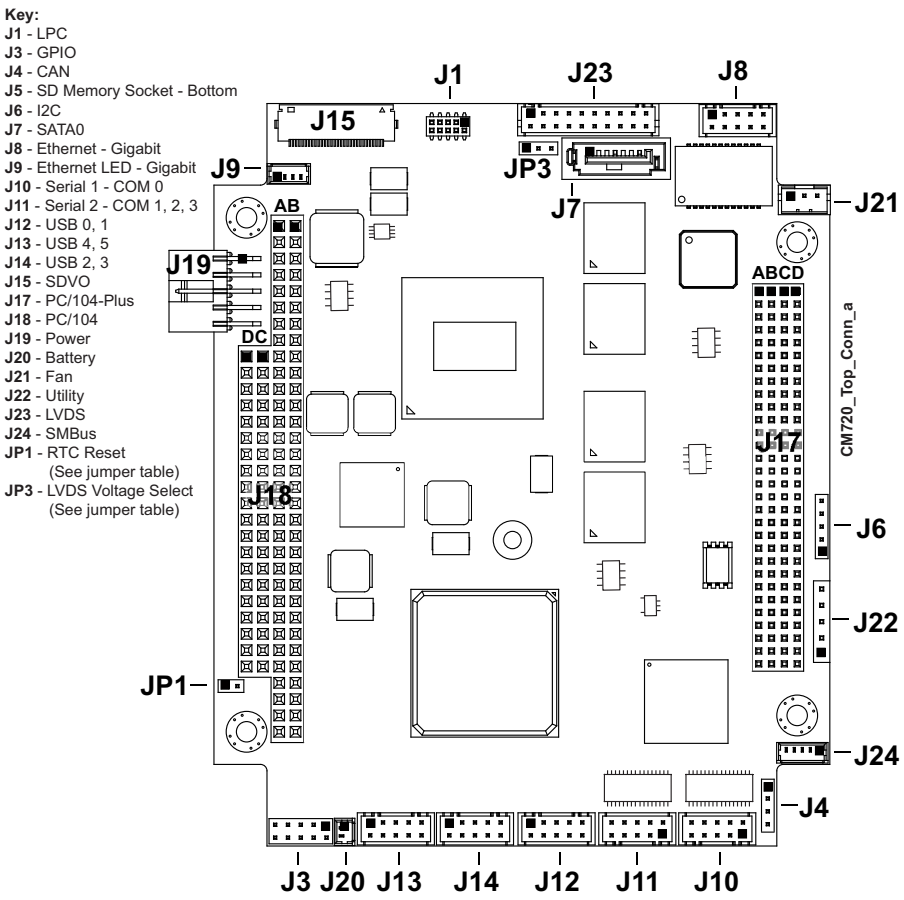

Figure 2-6. Header, Connector, and Socket Locations (Top Side)

NOTE Black square pins on headers and connectors represent pin 1. Black square pins on right-angle headers represent pin 2 in top-side views and pin 1 in bottom-side views.

Jumper Header Definitions

Table 2-3 describes the jumper headers shown in Figure 2-7. Both jumper headers provide 0.079" (2mm) pitch.

Table 2-3. Jumper Settings

Jumper Header	Installed	Removed
JP1 – Clear CMOS	Enable	Disable **(Default)**
JP3 – LVDS Voltage Selection	Enable +3.3V (1-2) **(Default)**	Enable +5V (2-3)

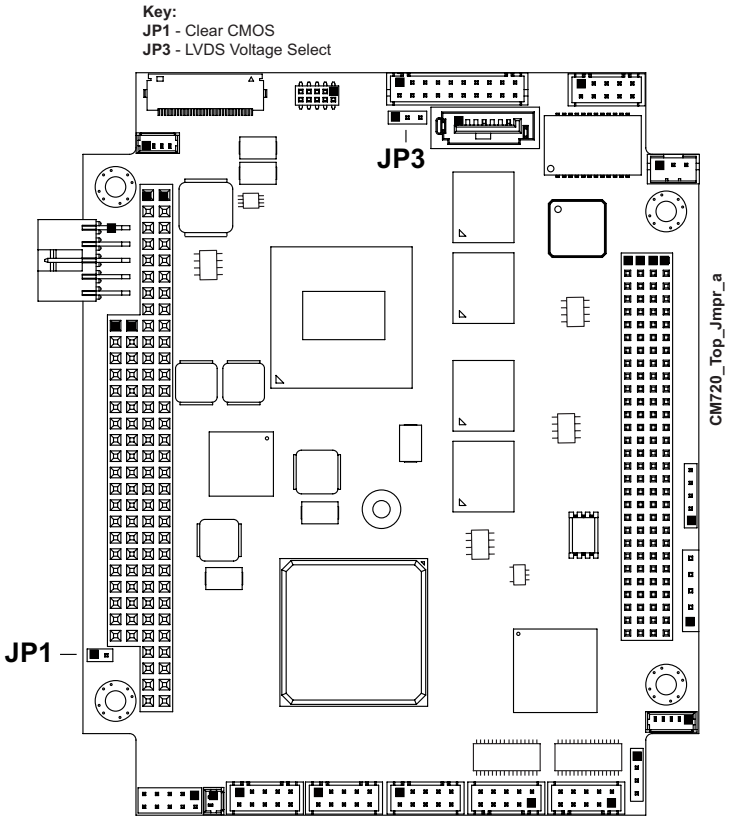

Figure 2-7. Jumper Header Locations (Top Side)

Specifications

Physical Specifications

Table 2-4 provides the physical dimensions of the CoreModule 720.

Table 2-4. Weight and Footprint Dimensions

Item	Dimension
Weight	0.12 kg (0.25 lbs)
Height (overall)	11.05 mm (0.435 inches)
Board thickness	2.362 mm (0.093 inches)
Width	96.01 mm (3.78 inches)
Length	115.57 mm (4.55 inches)

NOTE Height is measured from the upper board surface to the highest permanent component (PC/104 connector) on the upper board surface. This does not include the heatsink, which is required on all versions of the board but does not increase the height of the board. Component height should not exceed 0.345" (8.763mm) from the upper surface of the board and 0.190" (4.826mm) from the lower surface of the board. See Figure 2-9 on page 17 for the stack height of the heatsink on the board.

Mechanical Specifications

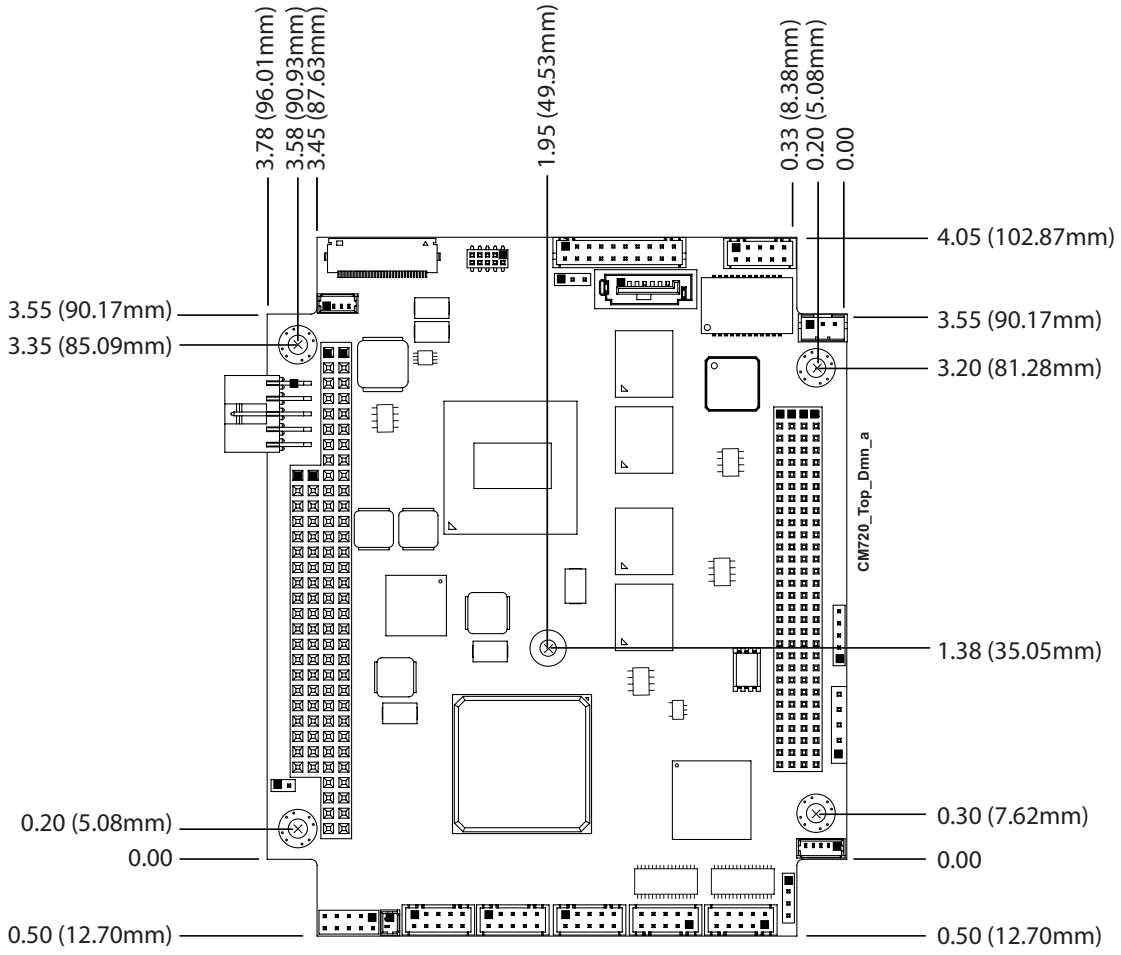

Figure 2-8. Mechanical Overview (Top Side)

NOTE	All dimensions are given in inches. Black square pins on headers and connectors represent pin 1. Black square pins on right-angle headers represent pin 2 in top-side views and pin 1 in bottom-side views.

Power Specifications

Table 2-5 provides the power requirements for the CoreModule 720.

Table 2-5. Power Supply Requirements

Parameter	600MHz E620T Characteristics	1.3GHz E660T Characteristics	1.6GHz E680T Characteristics
Input Type	Regulated DC voltages	Regulated DC voltages	Regulated DC voltages
Typical In-rush Current (Peak)	16.24A (81.20W)	16.24A (81.20W)	16.24A (81.20W)
Typical Idle Current	1.67A (8.34W)	1.69A (8.43W)	1.67A (8.33W)
BIT Current	2.72A (13.61W)	2.85A (14.25W)	2.97A (14.85W)

Operating configurations:

- In-rush operating configuration includes CRT monitor, 2GB memory, 8GB SSD, and power.
- Idle operating configuration includes In-rush configuration as well as one SATA hard drive, USB mouse and keyboard.
- BIT (Burn-In-Test) operating configuration includes Idle configuration as well as four USB loop backs, four serial ports with loop backs, and one Ethernet connection.

Environmental Specifications

Table 2-6 provides the most efficient operating and storage condition ranges required for this module.

Table 2-6. Environmental Requirements

Parameter	Conditions
Temperature	
Operating	–20° to +70° C (–4° to +158° F)
Extended (Optional)	–40° to +85° C (–40° to +185° F)
Storage	–55° to +85° C (–67° to +185° F)
Humidity	
Operating	5% to 90% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU is the primary source of heat on the board. The CoreModule 720 is designed to operate at the maximum speed of the CPU and requires a heatsink (provided). See Figure 2-9 for height measurements of the board and heatsink assembly.

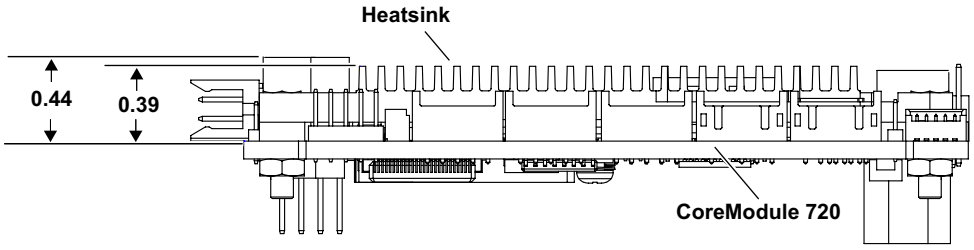

Figure 2-9. Stack Height of Cooling Assembly

NOTE	All heights are given in inches.

Chapter 3 Hardware

Overview

This chapter discusses the chips and connectors of the module features in the following order:

- CPU
- Graphics
- Memory
- Interrupt Channel Assignments
- Memory Map
- I/O Address Map
- Serial Port Interfaces
- USB Interfaces
- Ethernet Interface
- Video Interfaces
  - LVDS
  - SDVO
- Power Interface
- GPIO Interface
- Utility Interface
  - Power Button
  - Reset Switch
  - Speaker
- SMBus Interface
- CAN (Controller Area Network) Interface
- I^2C Interface
- System Fan Interface
- Battery Interface
- Ethernet LED Interface
- Miscellaneous
  - SSD (SATA Solid State Drive)
  - Time of Day/RTC
  - Oops! Jumper (BIOS Recovery)
  - Serial Console
  - Hot Cable
  - Watchdog Timer

NOTE ADLINK Technology, Inc. only supports the features and options listed in this manual. The main components used on the CoreModule 720 may provide more features or options than are listed in this manual. Some of these features and options are not supported on the module and will not function as specified in the chip documentation.

The pin-out tables only of non-standard headers and connectors are included in this chapter. This chapter does not include pin-out tables for standard headers, connectors, and sockets such as SATA, SD memory, PC/104, and PC/104-Plus. Refer to references in Chapter 1 for PC/104 and PC/104 Plus pin outs.

CPU

The CoreModule 720 offers three versions of the Intel Atom E6XXT CPU—the E620T, E660T, and E680T—operating at 600MHz, 1.3GHz, and 1.6GHz, respectively. The E6XXT integrates a high-performance x86 Processor Core with Memory Controller and 3D Graphics Engine. This single chip is based on 45-nm process technology and provides an open-standard PCI Express v1.0 interface, supporting user-defined PCH, ASIC, FPGA, and off-the-shelf discrete components, ideal for deeply embedded applications.

Graphics

The E6XXT CPU provides a 2D/3D graphics engine that performs pixel shading and vertex shading within a single hardware accelerator, which minimizes access to memory and improves render performance.

Memory

The CoreModule 720 employs two ranks of four system DRAM memory chips, which provide up to 2GB of extended memory, supporting aggressive power management to reduce power consumption, shallow self-refresh and a new deep self-refresh, proactive page closing policies to close unused pages, and partial writes through data mask pins.

Interrupt Channel Assignments

The interrupt channel assignments are shown in Table 3-1.

Table 3-1. Interrupt Channel Assignments

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
Secondary Cascade			X													
COM0				O	D											
COM1				D	O											
COM2											O	D				
COM3				O	O						D	O				
RTC									X							
Math Coprocessor														X		
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
USB	Automatically Assigned															
Video	Automatically Assigned															

Legend: D = Default, O = Optional, X = Fixed

> **NOTE** The IRQs for USB and Video are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

Memory Map

The following table provides the common PC/AT memory allocations. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table 3-2. Memory Map

Base Address			Function
00000000h	-	0009FFFFh	Conventional Memory
000A0000h	-	000AFFFFh	Graphics Memory
000B0000h	-	000B7FFFh	Mono Text Memory
000B8000h	-	000BFFFFh	Color Text Memory
000C0000h	-	000CFFFFh	Standard Video BIOS
000D0000h	-	000DFFFFh	DVMT Memory
000E0000h	-	000EFFFFh	PCI Express Base Memory
000F0000h	-	000FFFFFh	System Flash and PCI Resources

I/O Address Map

Table 3-3 shows the I/O address map. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
0000-00F	Primary DMA Controller0
0020-0021	Master Interrupt Controller
0040-0043	Programmable Interrupt Timer (Clock/Timer)
0060-006F	Keyboard Controller
0070-007F	CMOS RAM, NMI Mask Reg, RT Clock
0080-009F	DMA Page Registers
00A0-00BF	Slave Interrupt Controller
00C0-00DF	Slave DMA Controller #2
00F0-00FF	Math Coprocessor
02E8-02EF	Serial Port 4 (COM3)
02F8-02FF	Serial Port 2 (COM1)
03B0-03BB	Video (monochrome)
03C0-03DF	VGA
03E8-03EF	Serial Port 3 (COM2)
03F8-03FF	Serial Port 1 (COM0)
0400-041F	SMBus Configuration Ports
0500-053F	PCH GPIO Configuration Ports
0800-087F	PCH Power Management Ports
0A79h	ISA PnP Ports
0CF8-0CFF	PCI bus Configuration Address and Data

NOTE 0A79h is the ISA PnP port used by the BIOS and an OS that supports this feature to recognize ISA PnP (Plug and Play) cards.

The Intel I/O hub PCH EG20T does not support ISA DMA.

Serial Interfaces

The CoreModule 720 provides four RS-232 serial ports. The PCH EG20T contains the circuitry for all four serial ports and delivers the signals through two RS-232 transceivers: one transceiver for port COM0 and the second transceiver for ports COM1, COM2, and COM3. The serial ports support the following features:

- One individual high-speed NS16C550A-compatible UART (COM0)
- Programmable word length, stop bits, and parity
- 16-bit programmable baud rate generator and Interrupt generator
- Loop-back mode
- Four individual 16-bit FIFOs
- Serial Port Headers
  - J10 - Serial 1 (COM0) supports RS-232 and full modem
  - J11 - Serial 2 (COM1, COM2, and COM3) supports RS-232

Table 3-4 defines the pins and corresponding signals for serial 1 header (J10), which each consist of 10 pins, 2 rows, odd/even sequence (1, 2), and 0.079" (2mm) pitch.

Table 3-4. Serial 1 (COM0) Interface Pin Signal Descriptions (J10)

Pin #	Signal	DB9 Pin #	Description
1	S0_DCD*	1	COM0 Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake.
2	S0_DSR*	6	COM0 Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.
3	S0_RXD	2	COM0 Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS line to allow the transmission to complete.
4	S0_RTS*	7	COM0 Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control.
5	S0_TXD	3	COM0 Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line.
6	S0_CTS*	8	COM0 Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control.
7	S0_DTR*	4	COM0 Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness.
8	S0_RI*	9	COM0 Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	5	Ground
10	Key/NC	NC	Key Pin/Not connected

Note: The shaded table cell denotes ground.

Table 3-7 describes the pin signals of the serial 2 header (J11), which consists of 10 pins, two rows, odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch

Table 3-5. Serial 2 (COM1, 2, and 3) Interface Pin Signal Descriptions (J11)

Pin #	Signal	DB9 Pin #	Description
1	S1_TXD	3	COM1 Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent.
2	S1_RXD	2	COM1 Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted.
3	GND	5	Ground
4	S2_TXD	3	COM2 Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent.
5	S2_RXD	2	COM2 Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted.
6	GND	5	Ground
7	S3_TXD	3	COM3 Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent.
8	S3_RXD	2	COM3 Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted.
9	GND	5	Ground
10	GND	N/A	Ground

Note: The shaded table cells denote ground.

USB Interfaces

The CoreModule 720 contains three root USB hubs and six functional USB ports. The PCH provides the USB function including the following features:

- Supports USB v.2.0 EHCI and USB v.1.1 UHCI
- Provides over-current detection status
- Provides a fuse on board for over-current protection

Table 3-6 describes the pin signals of the USB0 and USB1 header which consists of 10 pins, in two rows, with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

Table 3-6. USB0 and USB1 Interface Pin Signals (J12)

Pin #	Signal	Description
1	USB-PWR_0	USB0 Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low.
2	USB-PWR_1	USB1 Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low.
3	CONN_USB0_N	USB0 Port Data Negative
4	CONN_USB1_N	USB1 Port Data Negative
5	CONN_USB0_P	USB0 Port Data Positive
6	CONN_USB1_P	USB1 Port Data Positive
7	USB_GND0	USB0 Ground
8	USB_GND1	USB1 Ground

Table 3-6. USB0 and USB1 Interface Pin Signals (J12) (Continued)

9	USB_GND0	USB0 Ground
10	USB_GND1	USB1 Ground

Note: The shaded table cells denote power or ground.

Table 3-7 describes the pin signals of the USB2 and USB3 header, which consists of 10 pins in two rows, with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

Table 3-7. USB2 and USB3 Interface Pin Signals (J14)

Pin #	Signal	Description
1	USB-PWR_2	USB2 Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low.
2	USB-PWR_3	USB3 Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low.
3	CONN_USB2_N	USB2 Port Data Negative
4	CONN_USB3_N	USB3 Port Data Negative
5	CONN_USB2_P	USB2 Port Data Positive
6	CONN_USB3_P	USB3 Port Data Positive
7	USB_GND2	USB2 Ground
8	USB_GND3	USB3 Ground
9	USB_GND2	USB2 Ground
10	USB_GND3	USB3 Ground

Note: The shaded table cells denote power or ground.

Table 3-8 describes the pin signals of the USB4 and USB5 header, which consists of 10 pins in two rows, with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

Table 3-8. USB4 and USB5 Interface Pin Signals (J13)

Pin #	Signal	Description
1	USB-PWR_4	USB4 Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low.
2	USB-PWR_5	USB5 Power – VCC (+5V +/-5%) power goes to the port through an on board fuse. Port is disabled if this input is low.
3	CONN_USB4_N	USB4 Port Data Negative
4	CONN_USB5_N	USB5 Port Data Negative
5	CONN_USB4_P	USB4 Port Data Positive
6	CONN_USB5_P	USB5 Port Data Positive
7	USB_GND4	USB4 Ground
8	USB_GND5	USB5 Ground
9	USB_GND4	USB4 Ground
10	USB_GND5	USB5 Ground

Note: The shaded table cells denote power or ground.

Ethernet Interface

The CoreModule 720 supports one Gigabit Ethernet interface. The Ethernet interface is implemented from the 82574IT Ethernet controller and provides oneGLAN interface, which occupies PCI Express port 2. The Ethernet function supports multi-speed operation at 10/100/1000 Mbps and operates in full-duplex at all supported speeds or half duplex at 10/100 Mbps while adhering to the IEEE 802.3x flow control specification. The Ethernet interface offers the following features:

- Full duplex or half duplex support at 10 Mbps, 100 Mbps, or 1000 Mbps
- In full duplex mode, the Ethernet controller adheres to the IEEE 802.3x Flow Control specification
- In half duplex mode, performance is enhanced by a proprietary collision reduction mechanism
- IEEE 802.3 compatible physical layer to wire transformer
- IEEE 802.3u Auto-Negotiation support
- Fast back-to-back transmission support with minimum interframe spacing (IFS)
- IEEE 802.3x auto-negotiation support for speed and duplex operation
- On-board magnetics (Ethernet isolation transformer)

Table 3-9 describes the pin signals of the Ethernet interface, which consists of a two-row, 10-pin shrouded header in two rows of odd/even (1,2) pin sequence, and 0.079" (2mm) pitch.

Table 3-9. Ethernet Interface Pin Signal Descriptions (J8)

Pin #	Signal	Description
1	GND	Ground
2	GND	
3	MDI0+	Media Dependent Interface 0 +/-
4	MDI0-	
5	MDI1+	Media Dependent Interface 1 +/-
6	MDI1-	
7	MDI2+	Media Dependent Interface 2 +/-
8	MDI2-	
9	MDI3+	Media Dependent Interface 3 +/-
10	MDI3-	

Note: The shaded table cells denote ground.

NOTE The magnetics (isolation transformer, T1) for the Ethernet connector is included on the CoreModule 720.

Video (SDVO/LVDS) Interfaces

The Atom™ E6XXT CPU provides an integrated 2D/3D graphics engine, which supports video decode such as MPEG2, MPEG4, VC1, WMV9, H.264 (main, baseline at L3 and High-profile level 4.0/4.1), and DivX* as well as video encode such as MPEG4, H.264 (baseline at L3), and VGA. The CPU supports LVDS and SDVO display ports, permitting simultaneous, independent operation of two displays. The video interface features are listed in the following bullets. Refer to Table 3-10 for definitions of the SDVO pin signals and Table 3-11 for the LVDS pin signal definitions.

SDVO:

- Supports a maximum resolution of 1280 x 1024 at 85Hz (pixel clock rate up to 160MHz)
- Supports a single channel interface through a 30-pin FPC connector
- Supports 100MHz to 160MHz derivative clock frequency
- Supports third-party output formats such as DVI, LVDS, HDMI, TV-Out, and VGA
- Provides a control bus able to operate at up to 1 MHz

LVDS:

- Supports a maximum resolution of 1280 x 768 at 60Hz (pixel clock rate up to 80MHz)
- Supports minimum pixel clock rate of 19.75MHz
- Supports a single channel interface through a 20-pin header
- Supports pixel color depths of 18 and 24 bits
- Supports 20MHz to 80MHz derivative clock frequency

Table 3-10 lists the pin signals of the SDVO FPC connector, which provides 30 pins in a single row with 0.020" (0.5mm) pitch.

Table 3-10. SDVO Interface Pin Signals (J15)

Pin #	Signal	Description
1	GND1	Ground 1
2	SDVOB_CLK-	SDVO B Clock Negative
3	SDVOB_CLK+	SDVO B Clock Positive
4	GND2	Ground 2
5	SDVOB_GREEN-	SDVO B GREEN Negative
6	SDVOB_GREEN+	SDVO B GREEN Positive
7	GND3	Ground 3
8	SDVOB_INT-	SDVO B Input Interrupt Negative
9	SDVOB_INT+	SDVO B Input Interrupt Positive
10	GND4	Ground 4
11	SDVOB_BLU-	SDVO B BLUE Negative
12	SDVOB_BLU+	SDVO B BLUE Positive
13	GND5	Ground 5
14	SDVOB_RED-	SDVO B RED Negative
15	SDVOB_RED+	SDVO B RED Positive
16	GND6	Ground 6
17	SDVO_FLDSTALL-	SDVO Input Field Stall Negative
18	SDVO_FLDSTALL+	SDVO Input Field Stall Positive
19	GND7	Ground 7

Table 3-10. SDVO Interface Pin Signals (J15) (Continued)

Pin #	Signal	Description
20	SDVO_I2C_CLK	I2C control signal (Clock) for SDVO device
21	SDVO_I2C_DAT	I2C control signal (Data) for SDVO device
22	RESET	Reset signal
23	+3.3V_1	+3.3 Volt Power 1
24	+2.5V	+2.5 Volt Power
25	+5V_1	+5 Volt Power 1
26	GND8	Ground 8
27	SDVO_TVCLKIN-	SDVO TV-Out Synchronization Clock Input - Negative
28	SDVO_TVCLKIN+	SDVO TV-Out Synchronization Clock Input - Positive
29	+3.3V_2	+3.3 Volt Power 2
30	+5V_2	+5 Volt Power 2

Note: The shaded table cells denote power or ground.

Table 3-10 lists the pin signals of the LVDS video header, which provides 20 pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-11. LVDS Video Interface Pin Signals (J23)

Pin #	Signal	Description
1	+12V	+12 volts for flat panel and backlight
2	VCC_LVDS_CONN	JP3 determines LVDS voltage (+3.3V or +5V)
3	GND	Ground
4	GND	Ground
5	LVDSA_CLK_P	LVDS A Clock Positive
6	LVDSA_CLK_N	LVDS A Clock Negative
7	LVDSA_DAT3_P	LVDS A DATA Positive Line 3
8	LVDSA_DAT3_N	LVDS A DATA Negative Line 3
9	LVDSA_DAT2_P	LVDS A DATA Positive Line 2
10	LVDSA_DAT2_N	LVDS A DATA Negative Line 2
11	LVDSA_DAT1_P	LVDS A DATA Positive Line 1
12	LVDSA_DAT1_N	LVDS A DATA Negative Line 1
13	LVDSA_DAT0_P	LVDS A DATA Positive Line 0
14	LVDSA_DAT0_N	LVDS A DATA Negative Line 0
15	LBKLT_CTL	Panel Backlight Control
16	LVDD_EN	Enable Panel Power
17	LDDC_CLK	Display Data Channel Clock
18	LDDC_DATA	Display Data Channel Data
19	LBKLT_EN	Enable Backlight Inverter
20	NC	Not Connected

Note: The shaded table cells denote power or ground.

Power Interface

The CoreModule 720 requires one +5 volt DC power source and provides a shrouded 10-pin, right-angle header with 2 rows, odd/even pin sequence (1, 2), and 0.100" (2.54mm) pitch. If the +5VDC power drops below ~4.65V, a low voltage reset is triggered, resetting the system.

The power input header (J19) supplies the following voltage and ground directly to the module:

- 5.0VDC +/- 5%

Table 3-12. Power Interface Pin Signals (J19)

Pin	Signal	Descriptions
1	GND	Ground
2	+5V	+5 Volts
3	GND	Ground
4	+12V	+12 Volts routed to PC/104, PC/104-Plus, and LVDS interfaces
5	GND	Ground
6	+3.3V_PCI	+3.3 Volts routed to PCI
7	GND	Ground
8	+5V	+5 Volts
9	GND	Ground
10	+5V	+5 Volts

Note: The shaded table cells denote power or ground.

User GPIO Interface

The CoreModule 720 provides GPIO pins for customer use, routing the signals from the PCH EG20T chipset to the J3 header. An example test application and source code reside in each BSP directory of the CoreModule 720 Support Software QuickDrive.

For instructions on using the example applications, refer to the GPIO Readme in each BSP directory of the QuickDrive. For more information about the GPIO pin operation, refer to the PCH EG20T datasheet at:

http://download.intel.com/embedded/chipsets/datasheet/324211.pdf

Table 3-13 describes the pin signals of the GPIO interface, which consists of a 10-pin header with 2 rows, odd/even pin sequence (1, 2), and 0.079" (2mm) pitch.

Table 3-13. User GPIO Interface Pin Signals (J3)

Pin #	Signal from PCH	Description
1	GPIO0	User defined
2	GPIO4	User defined
3	GPIO1	User defined
4	GPIO5	User defined
5	GPIO2	User defined
6	GPIO6	User defined
7	GPIO3	User defined
8	GPIO7	User defined
9	GND	Ground
10	GND	Ground

Note: The shaded table cells denote ground.

Utility Interface

The Utility interface provides three I/O signals on the module and consists of a 5-pin, 0.100" (2.54mm), single-row header (J22). The E6XXT CPU drives the Power Button and Speaker signals on the Utility interface. A separate Power Management microprocessor drives the Reset Switch signal. Table 3-14 provides the signal definitions.

- Power Button
- Reset Switch
- Speaker

Power Button

The Utility header provides a signal for an external Power Button through pins 1 and 2. The Power Button allows the user to shut down and power on the system. To shut down the system, press and hold the Power Button for four seconds. Press the Power Button for one second to power on the system.

Reset Switch

Pins 2 and 3 on the Utility header provide the signal for an external reset button, which allows the user to re-boot the system.

Speaker

The speaker signal provides sufficient signal strength to drive an external 1W 8 Ω “Beep” speaker at an audible level through pins 4 and 5 on the Utility header. The speaker signal is driven from an on-board amplifier and the CPU.

Table 3-14 describes the pin signals of the Utility interface, which provides a 5-pin, single-row header with 0.100" (2.54mm) pitch.

Table 3-14. Utility Interface Pin Signals (J22)

Pin #	Signal	Description
1	PWR_BTN*	External Power Button (Pins 1-2)
2	GND	Ground
3	RESET SW*	External Reset Switch signal (Pins 2-3)
4	5V	+5 Volts Power
5	SPKR_CONN	Speaker Output (Pins 4-5)

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

System Management Bus (SMBus)

The E6XXT chip contains a host SMBus port. The host port allows the CPU access to the SMBus slaves through header, J24. The SMBus slaves include the Gigatbit Ethernet Controller and the CPU Temperature Monitor. Table 3-15 lists the device names and corresponding reserved binary addresses on the SMBus. Table 3-16 lists the SMBus pin signals on 5 pins, 1 row, 0.079" (2mm) pitch.

Table 3-15. SMBus Reserved Addresses

Component	Address (Binary)
CPU Temperature Monitor	$1001,100x_b$
Gigabit Ethernet Controller	$1100,001x_b$

Table 3-16. SMBus Pin Signals (J24)

Pin #	Signal	Description
1	SMB_CLK	SMBus Clock
2	GND	Ground
3	SMB_DATA	SMBus Data
4	VSM	+3.3V standby voltage
5	SMB_ALERT*	SMBus Alert

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

CAN Bus Interface

The CAN controller resides in the PCH and performs communication in accordance with the Bosch CAN Protocol version 2.0B Active (standard and extended formats.) The CAN transceiver connects the CAN controller to the CAN bus, and transmits and receives CAN signals to and from the CAN header (J4). The CAN interface delivers CAN signals used for automotive, industrial automation, and medical scanning and imaging applications. The following list describes some of the features of the CAN Bus Interface.

- +/- 12 kV ESD protection
- Low-current Standby mode with bus wake up: 5µA typical
- Bus-fault protection of -27V to 40V
- Over-temperature shutdown

Table 3-14 defines the pin signals of the CAN bus interface, which provides a 4-pin, single-row header with 0.079" (2mm) pitch.

Table 3-17. CAN Interface Pin Signals (J4)

Pin #	Signal	Description
1	CAN_L	Dominant Low
2	CAN_H	Dominant High
3	+5V	+5 volts power
4	GND	Ground

Note: The shaded table cells denote power or ground.

I²C Interface

The CoreModule 720 provides a single-channel I2C interface, which conforms to version 2.1 of the I2C bus specification. The I2C controller resides on the EG20T PCH and operates as a master or slave device, supporting a multi-master bus. The following list highlights the features of the I2C bus interface.

- Supports delay processing of data read/write operation
- Supports master and slave devices
- Supports SCL generation when acting as a clock master
- Supports multiple masters
- Supports Low-Speed BusClock as its clock source and generates an SCL clock based on the set value of the I2CBC register
- Supports 32-byte buffering
- Provides a function that generates time out in buffer mode

Table 3-14 defines the pin signals of the I²C bus interface, which provides a 5-pin, single-row header with 0.079" (2mm) pitch.

Table 3-18. I²C Interface Pin Signals (J6)

Pin #	Signal	Description
1	I2C_CLK	I2C Clock
2	GND	Ground
3	I2C_DATA	I2C Data
4	+3.3V	+3.3 volts power
5	NC	Not Connected

Note: The shaded table cells denote power or ground.

System Fan

Table 3-19 lists the pin signals of the System Fan header, which provides a single row of 3 pins with 0.079" (2mm) pitch.

Table 3-19. System Fan Pin Signals (J21)

Pin #	Signal	Description
1	+V_FAN	+5.0 volts DC +/- 5%
2	NC	Not Connected
3	GND	Ground

Note: The shaded table cells denote power or ground.

Battery

Table 3-20 lists the pin signals of the External Battery Input header for backup CMOS RAM and RTC (Real Time Clock), which uses 2 pins, in a single row, with 0.049" (1.25mm) pitch.

Table 3-20. External Battery Input Header (J20)

Pin #	Signal	Description
1	VBAT_EXT	+3.3 volts DC +/- 5%
2	GND	Ground

Note: The shaded table cells denote power or ground.

Ethernet External LED

This header provides signals for an external LED that indicates Ethernet links and activity using a single row of 4 pins with 0.049" (1.25mm) pitch.

Table 3-21. Ethernet External LED Pin Signals (J9)

Pin #	Signal	Description
1	V3.3_CONN	+3 volts – Provides +3 volts to external LED (Pins 1-2 for Green LED)
2	ETH_ACT_LED	Ethernet Activity
3	ETH_LINK100_LED	Fast Ethernet Link with +3 volts power (Pins 3-4 for Bi-Color LED)
4	ETH_LINK1000_LED	Gigabit Ethernet Link

Note: The shaded table cell denotes power.

Miscellaneous

SSD (Solid State Drive)

The CoreModule 720 provides an 8GB SATA SSD, which is soldered directly onto the board. For more information refer to the SSD data sheet: http://www.greenliant.com/dotAsset/45628.pdf.

Real Time Clock (RTC)

The CoreModule 720 contains a Real Time Clock (RTC). The RTC can be backed up with a battery. If the battery is not present, the board BIOS has a battery-less boot option to complete the boot process.

Oops! Jumper (BIOS Recovery)

The Oops! jumper function is provided in the event the BIOS settings you have selected prevent you from booting the system. By using the Oops! jumper you can prevent the current BIOS settings in flash from being loaded, allowing you to boot using default settings.

Use a jumper to connect the DTR pin (4) to the RI pin (9) on Serial Port 1 (COM0) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and return to BIOS Setup. You must now load factory defaults by selecting *Restore Defaults* from the *Save & Exit* menu. Then select *Save Changes and Exit* to reboot the system. Now you can modify the default settings to your desired values. Ensure you save the changes before rebooting the system.

To convert a standard DB9 connector to an Oops! jumper, short together the DTR (4) and RI (9) pins on the front of the connector as shown in Figure 3-1 on the Serial Port 1 DB9 connector.

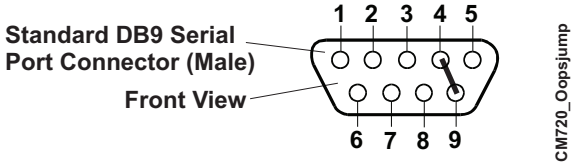

Figure 3-1. Oops! Jumper Serial Port (DB9)

Serial Console

The CoreModule 720 BIOS supports the serial console (or console redirection) feature. This I/O function is ANSI-compatible with a serial terminal or with equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Serial Console Setup

The serial console feature is implemented by entering the serial console settings in the BIOS Setup Utility and connecting the appropriate serial cable (a standard null modem serial cable or "Hot Cable") between one of the serial ports (COM0) and the serial terminal or a PC with communications software.

Hot (Serial) Cable

To convert a standard serial cable to a "Hot Cable", short together the RTS (7) and RI (9) pins on the serial port DB9 connector as shown in Figure 3-2.

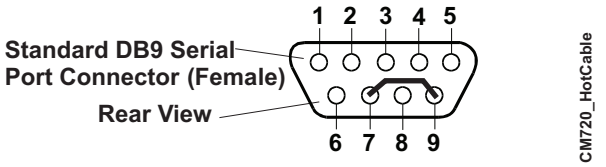

Figure 3-2. Serial Console Jumper

Watchdog Timer

The Watchdog Timer (WDT) restarts the system if a mishap occurs, ensuring proper start up after the interruption. Possible problems include failure to boot properly, the application software's loss of control, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (Watchdog Timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT using *Watchdog Timer* of the Boot menu in BIOS Setup. Set the WDT for a time-out interval in seconds, between 0 and 600, in one-second increments in the Boot Configuration screen. Ensure you allow enough time for the boot process to complete and for the OS to boot. The OS or application must tickle the WDT as soon as it comes up. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some ADLINK Board Support Packages provide an API interface to the WDT. The application must tickle the WDT in the time set when the WDT is initialized or the system will be reset. You can use a BIOS call to tickle the WDT or access the hardware directly.

- Watchdog Code examples – ADLINK has provided source code examples on the CoreModule 720 Support Software QuickDrive illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file on the CoreModule 720 Support Software QuickDrive.

Chapter 4 BIOS Setup

Introduction

This section assumes the user is familiar with general BIOS Setup and does not attempt to describe the BIOS functions. Refer to "BIOS Setup Menus " on page 37 in this chapter for a map of the BIOS Setup settings. If ADLINK has added to or modified any of the standard BIOS functions, these functions will be described.

Entering BIOS Setup (Local Video Display)

To enter BIOS Setup using a local video display for the CoreModule 720:

1. Turn on the display and the power supply to the CoreModule 720.
2. Start Setup by pressing the [Del] or [F2] keys (F2 allows you to load previous settings) when the following message appears on the boot screen.

```
Please wait. This will take a few seconds.
```

> **NOTE** If the setting for *Fast Boot* is [Enabled], the system may not enter the BIOS set up if you do not press the <Del> or <F2> keys early in the boot sequence.

3. Follow the instructions on the right side of the screen to navigate through the selections and modify any settings.

Entering BIOS Setup (Serial Port Console)

This section describes how to enter the BIOS setup through a remote serial terminal or PC.

1. Turn on the power supply to the CoreModule 720 and enter the BIOS Setup Utility using a local video display.
2. Ensure the BIOS feature *Serial Port Console Redirection* is set to [Enabled] under the **Advanced** menu.
3. Accept the default options or make your own selections for the balance of the Console Redirection fields and record your settings.
4. Ensure you select the type of remote serial terminal you will be using and record your selection.
5. Select *Save Changes and Exit* and then shut down the CoreModule 720.
6. Connect the remote serial terminal (or the PC with communications software) to the COM0 serial port on the CoreModule 720.
7. Turn on the remote serial terminal or PC and set it to the settings you selected in the earlier in the procedure.

   The default settings for the CoreModule 720 are:

   - ANSI
   - 115200
   - 8 bits
   - no parity
   - 1 stop bit
   - no flow control (None)
   - Disabled Recorder Mode
   - Disabled Resolution 100x31
   - [80x24] for Legacy OS Redirection

8. Restore power to the CoreModule 720.
9. Press the F2 key to enter Setup (early in the boot sequence if *Fast Boot* is set to [Enabled].)

   If *Fast Boot* is set to [Enabled], you may never see the screen prompt.
10. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.

> **NOTE** The serial console port is not hardware protected. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

OEM Logo Utility

The CoreModule 720 BIOS supports a graphical logo utility, which allows the user to customize the boot screen image. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image on screen during the boot process and remain there while the OS boots, depending on the options selected in BIOS Setup.

> **NOTE** The Quiet Boot feature must be set to Enabled in the Boot screen of BIOS Setup for the system to recognize the OEM Logo feature.

Logo Image Requirements

Please contact your ADLINK Sales Representative for more information on OEM Logo Utility requirements.

BIOS Setup Menus

This section provides illustrations of the six main setup screens in the CoreModule 720 BIOS Setup Utility. Below each illustration is a bullet list of the screen's submenus and setting selections. The setting selections are presented in brackets after each submenu or menu item, and the optimal default settings are presented in bold. For more detailed definitions of the BIOS settings, refer to the AMI Aptio TSE User Manual: http://www.ami.com/support/doc/AMI_TSE_User_Manual_PUB.pdf.

Table 4-1. BIOS Setup Menus

BIOS Setup Utility Menu	Item/Topic
Main	Language, Date, and Time
Advanced	Launch PXE OpROM, Launch Storage OpROM, PCI Subsystem, CPU, GPIO, Thermal, SDIO, USB, Hardware Monitor, Serial Port Console
Chipset	North Bridge and South Bridge configurations
Boot	Boot up Settings, Boot Options, Boot Order
Security	Setting or changing Passwords
Save & Exit	Exiting with or without changing settings, loading and restoring Optimal or User Defaults

Main BIOS Setup Screen

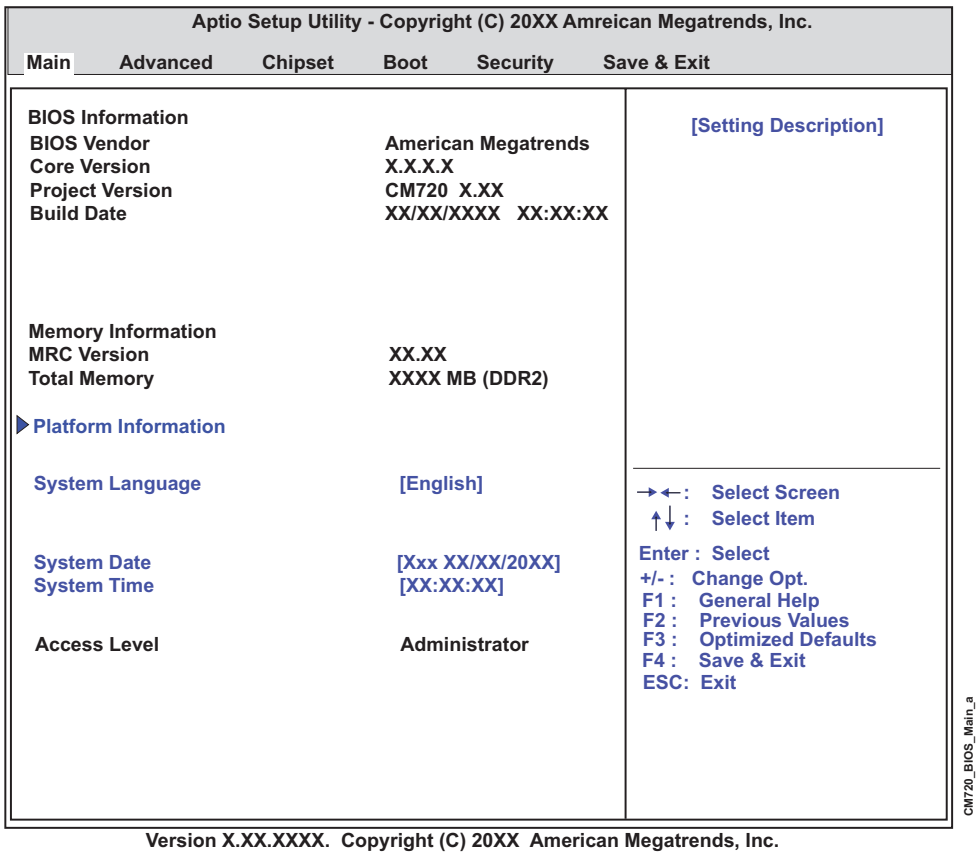

Figure 4-1. Main BIOS Setup Screen

- **Platform Information**
  - Tunnel Creek Version XX (XX Stepping)
  - PUNIT Build Date Xxx XX 20XX
  - PUNIT Build Time X:XX:XX

- **System Language** **[English]**
- **System Date**

  System Date (day of week, mm:dd:yyyy) – This field requires the alpha-numeric entry of the day of week, day of the month, calendar month, and all 4 digits of the year, indicating the century plus year (*Fri XX/XX/20XX*).

- **System Time**

  System Time (hh:mm:ss) – This is a 24-hour clock setting in hours, minutes, and seconds.

Advanced BIOS Setup Screen

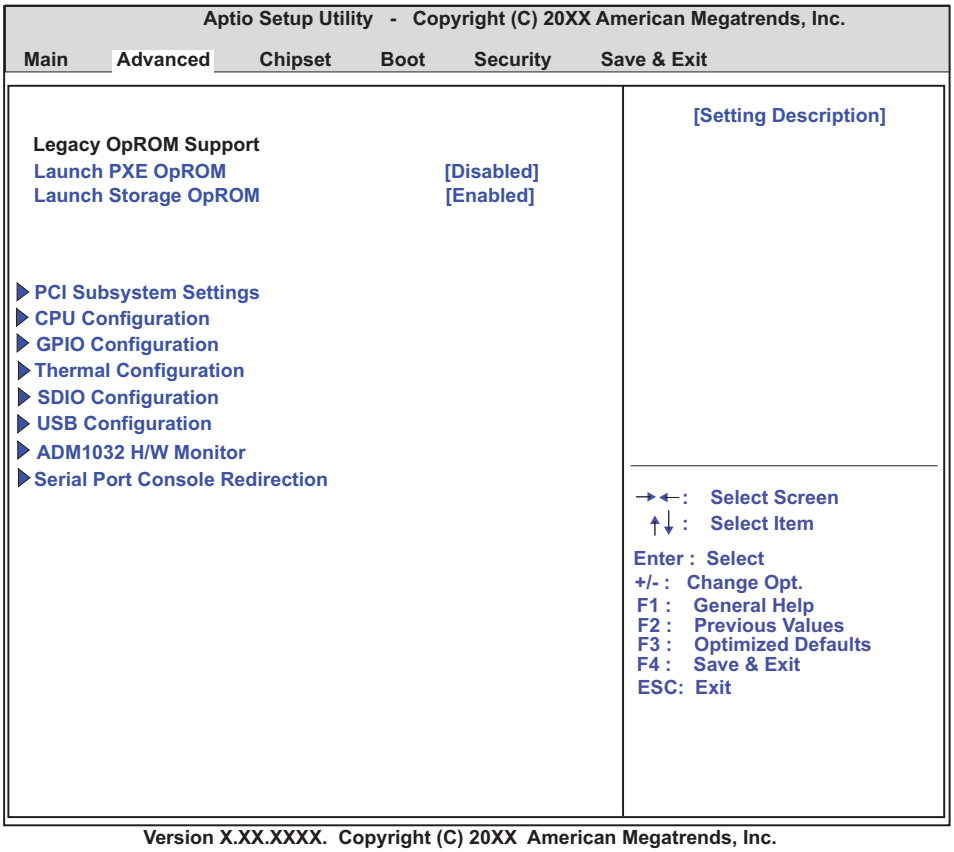

Figure 4-2. Advanced BIOS Setup Screen

- **Legacy OpROM Support**
  - Launch PXE OpROM [**Disabled**; Enabled]
  - Launch Storage OpROM [Disabled; **Enabled**]
- **PCI Subsystem Settings**
  - PCI Bus Driver Version V X.XX.XX
    - PCI ROM Priority [64 PCI Bus Clock; **EFI Compatible ROM**]
  - PCI Common Settings
    - PCI Latency Timer [**32 PCI Bus Clocks**; 64 PCI Bus Clocks; 96 PCI Bus Clocks; 128 PCI Bus Clocks; 160 PCI Bus Clocks; 192 PCI Bus Clocks; 224 PCI Bus Clocks; 248 PCI Bus Clocks]

- VGA Palette Snoop [**Disabled**; Enabled]
- PERR# Generation [**Disabled**; Enabled]
- SERR# Generation [**Disabled**; Enabled]

♦ PCI Express Device Settings

- Relaxed Ordering [**Disabled**; Enabled]
- Extended Tag [**Disabled**; Enabled]
- No Snoop [Disabled; **Enabled**]
- Maximum Payload [**Auto**; 128 Bytes; 256 Bytes; 512 Bytes; 1024 Bytes; 2048 Bytes; 4096 Bytes]
- Maximum Read Request [**Auto**; 128 Bytes; 256 Bytes; 512 Bytes; 1024 Bytes; 2048 Bytes; 4096 Bytes]

♦ PCI Express Link Settings

- Automatic ASPM [**Disabled**; Auto; Force L0]
  WARNING: Enabling ASPM may cause some PCI-E devices to fail
- Extended Synch [**Disabled**; Enabled]

• **CPU Configuration**

♦ Processor Type Genuine Intel(R) CPU
♦ EMT64 Supported
♦ Processor Speed XXXX MHz
♦ Ratio Status XX
♦ Actual Ratio XX
♦ System Bus Speed XXX MHz
♦ Processor Stepping XXXXX
♦ Microcode Revision XXX
♦ L1 Cache RAM XX k
♦ L2 Cache RAM XXX k
♦ Processor Core Single
♦ Hyper-Threading Supported

♦ Intel SpeedStep [Disabled; **Enabled**]
♦ Hyper-Threading [Disabled; **Enabled**]
♦ Execute Disable Bit [Disabled; **Enabled**]
♦ Limit CPUID Maximum [**Disabled**; Enabled]
♦ Intel Virtualization [**Disabled**; Enabled]
♦ C-States [Disabled; **Enabled**]
♦ Enhanced C1 [**Disabled**; Enabled]
♦ Enhanced C2 [Disabled; **Enabled**]
♦ Enhanced C3 [**Disabled**; Enabled]
♦ Enhanced C4 [Disabled; **Enabled**]

- GPIO Configuration
  - GPIO 0 [**Disabled**; Enabled]
  - GPIO 1 [**Disabled**; Enabled]
  - GPIO 2 [**Disabled**; Enabled]
  - GPIO 3 [**Disabled**; Enabled]
  - GPIO 4 [**Disabled**; Enabled]
  - GPIO 5 [**Disabled**; Enabled]
  - GPIO 6 [**Disabled**; Enabled]
  - GPIO 7 [**Disabled**; Enabled]
  - GPIO 8 [**Disabled**; Enabled]
  - GPIO 9 [**Disabled**; Enabled]
  - GPIO 10 [**Disabled**; Enabled]
  - GPIO 11 [**Disabled**; Enabled]
- **Thermal Configuration**
  - Critical Trip Point [**POR**; 30 C; 40 C; 50 C; 60 C; 70 C; 80 C; 90 C; 95 C]
  - Active Trip Point [Disabled; 30 C; 40 C; 50 C; **60 C**; 70 C; 80 C; 90 C; 95 C; 100 C]
  - Passive Trip Point [Disabled; 30 C; 40 C; 50 C; 60 C; **70 C**; 80 C; 90 C; 95 C; 100 C]
    - Passive TC1 Value [**1**]
    - Passive TC2 Value [**5**]
    - Passive TSP Value [**10**]
  - Thermal Offset [**Disabled**; Enabled]
  - DTS Calibration [Disabled; **Enabled**]
- **SDIO Configuration**
  - SDIO Access Mode [**Auto**; DMA; PIO]
- **USB Configuration**
  - USB Devices:

    1 Keyboard
    - Legacy USB Support [Disabled; **Enabled**]
    - EHCI Hand-off [**Disabled**; Enabled]
  - USB hardware delays and time-outs:
    - USB transfer time-out [1 sec; 5 sec; 10 sec; **20 sec**]
    - Device reset time-out [10 sec; **20 sec**; 30 sec; 40 sec]
    - Device power-up delay [**Auto**; Manual]
- **ADM1032 H/W Monitor**
  - CPU Health Status
    - CPU Temp : +XX
- Serial Port Console Redirection
  - COM0 (Pci Bus2, Dev10, Func1)
    - Console Redirection [Disabled; **Enabled**]

- Console Redirection Settings
  - Terminal Type [VT100; VT100+; VT-UTF8; **ANSI**]
  - Bits per second [9600; 19200; 38400; 57600; **115200**]
  - Data Bits [7; **8**]
  - Parity [**None**; Even; Odd; Mark; Space]
  - Stop Bits [**1**; 2]
  - Flow Control [**None**; Hardware RTS/CTS]
  - Recorder Mode [**Disabled**; Enabled]
  - Resolution 100x31 [**Disabled**; Enabled]
  - Legacy OS Redirection [**80x24**; 80x25]

  .

NOTE	The serial port console is not hardware protected. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

Chipset BIOS Setup Screen

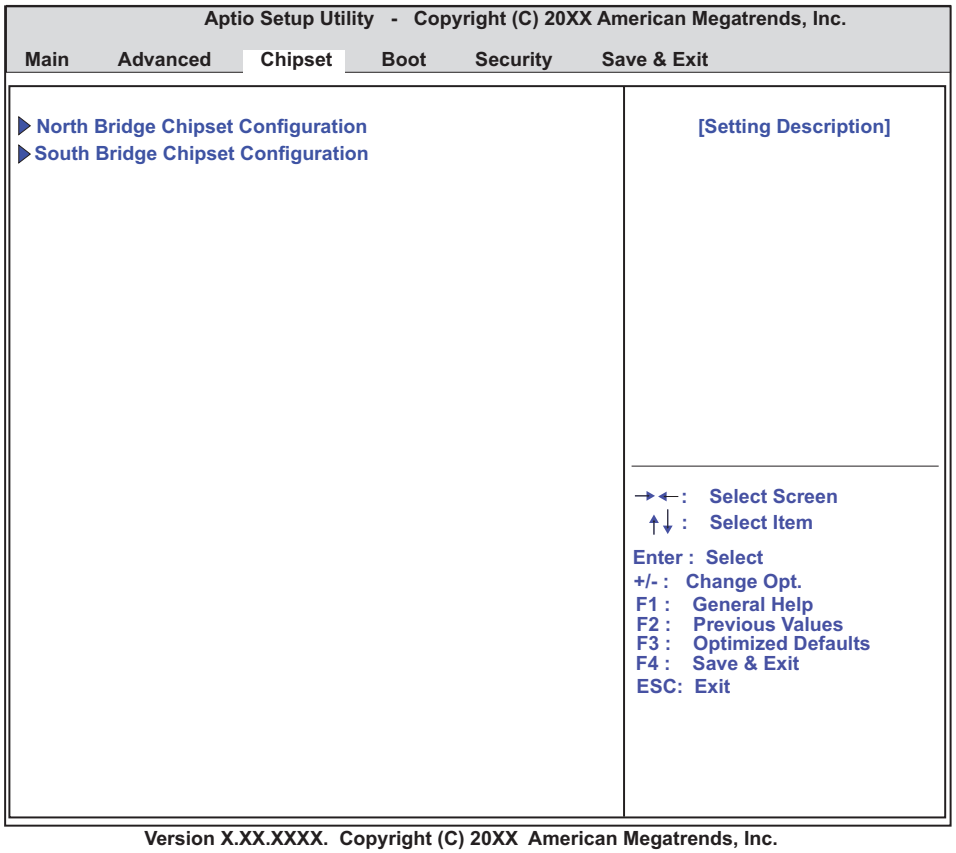

Figure 4-3. Chipset BIOS Setup Screen

- North Bridge Chipset Configuration
  - Memory Information
    - MRC Version XX.XX
    - Total Memory XXXX MB (DDR2)

- vBIOS Version XXXX
- IEGD Driver Version N/A

♦ IGD Mode Select [Disabled;
Enabled, 1MB;
Enabled, 4MB;
Enabled, 8MB;
Enabled, 16MB;
Enabled, 32MB;
Enabled, 48MB;
Enabled, 64MB]

♦ MSAC Mode Select [Enabled, 512MB;
Enabled, 256MB;
Enabled, 128MB]

♦ Boot Display Configuration
- Boot Display Device [Integrated LVDS; **External DVI/HDMI**]
- Flat Panel Scaling [**Auto**; Forced; Disabled]
- Flat Panel Type [640x480 18bit;
800x600 18bit;
1024x600 18bit;
1024x768 18bit;
1280x768 18bit;
640x480 24bit;
800x600 24bit;
1024x600 24bit;
1024x768 24bit;
1280x768 24bit]

• **South Bridge Chipset Configuration**

♦ SMBUS Controller [**Enabled**; Disabled]

♦ High Precision Event Timer Configuration
- High Precision Timer [Disabled; **Enabled**]

♦ PPM Config
- C-state POPUP [Disabled; **Enabled**]

Boot BIOS Setup Screen

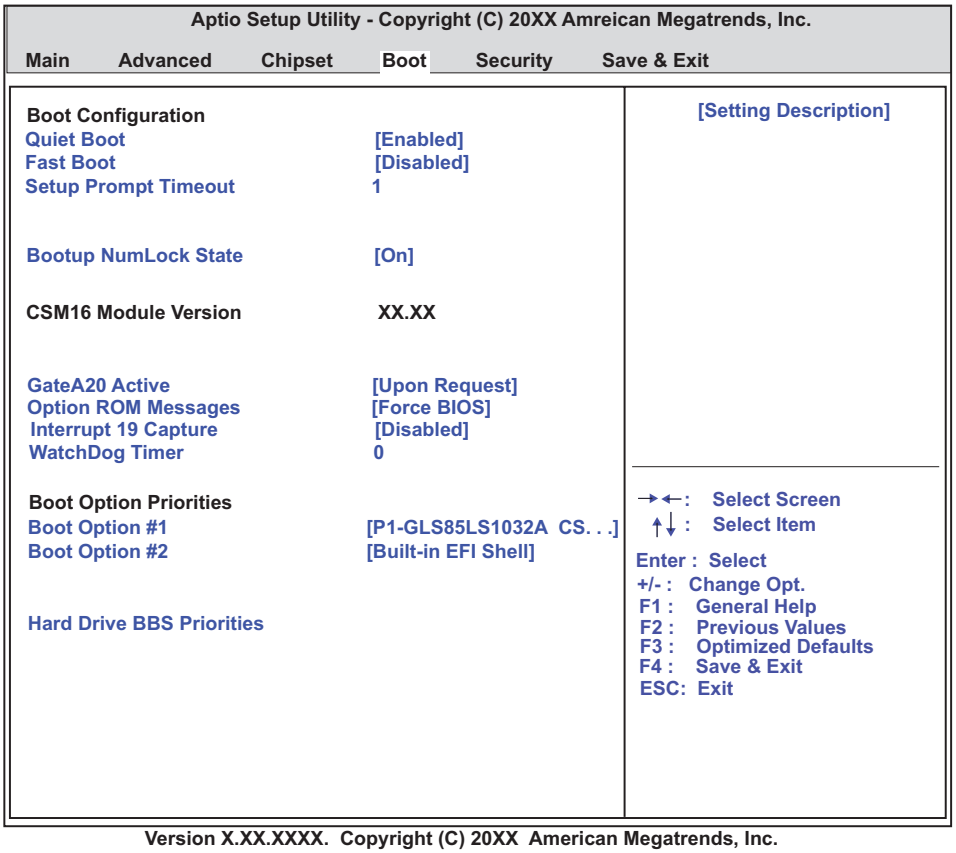
Aptio Setup Utility - Copyright (C) 20XX Amreican Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Boot Configuration
Quiet Boot [Enabled]
Fast Boot [Disabled]
Setup Prompt Timeout 1
Bootup NumLock State [On]
CSM16 Module Version XX.XX
GateA20 Active [Upon Request]
Option ROM Messages [Force BIOS]
Interrupt 19 Capture [Disabled]
WatchDog Timer 0
Boot Option Priorities
Boot Option #1 [P1-GLS85LS1032A CS. . .]
Boot Option #2 [Built-in EFI Shell]
Hard Drive BBS Priorities
[Setting Description]
→←: Select Screen
↑↓: Select Item
Enter : Select
+/- : Change Opt.
F1 : General Help
F2 : Previous Values
F3 : Optimized Defaults
F4 : Save & Exit
ESC: Exit
Version X.XX.XXXX. Copyright (C) 20XX American Megatrends, Inc.
CM720_BIOS_Boot_a

Figure 4-4. Boot BIOS Setup Screen

- **Boot Configuration**
  - Quiet Boot [Disabled; **Enabled**]
  - Fast Boot [**Disabled**; Enabled]
  - Setup Prompt Timeout [**1**]
  - Bootup NumLock State [**On**; Off]
- **CSM16 Module Version XX.XX**
  - Gate A20 Active [**Upon Request**; Always]
  - Option ROM Messages [**Force BIOS**; Keep Current]
  - Interrupt 19 Capture [**Disabled**; Enabled]
  - WatchDog Timer [**0**]
- **Boot Option Priorities**
  - Boot Option #1 [**P1-GLS85LS1032A CS 32GBN A101C0**; Built -in EFI Shell; Disabled]
  - Boot Option #2 [P1-GLS85LS1032A CS 32GBN A101C0; **Built-in EFI Shell**; Disabled]
  - Hard Drive BBS Priorities
    - Boot Option #1 [**P1-GLS85LS1032A CS 32GBN A101C0**; Disabled]

Security BIOS Setup Screen

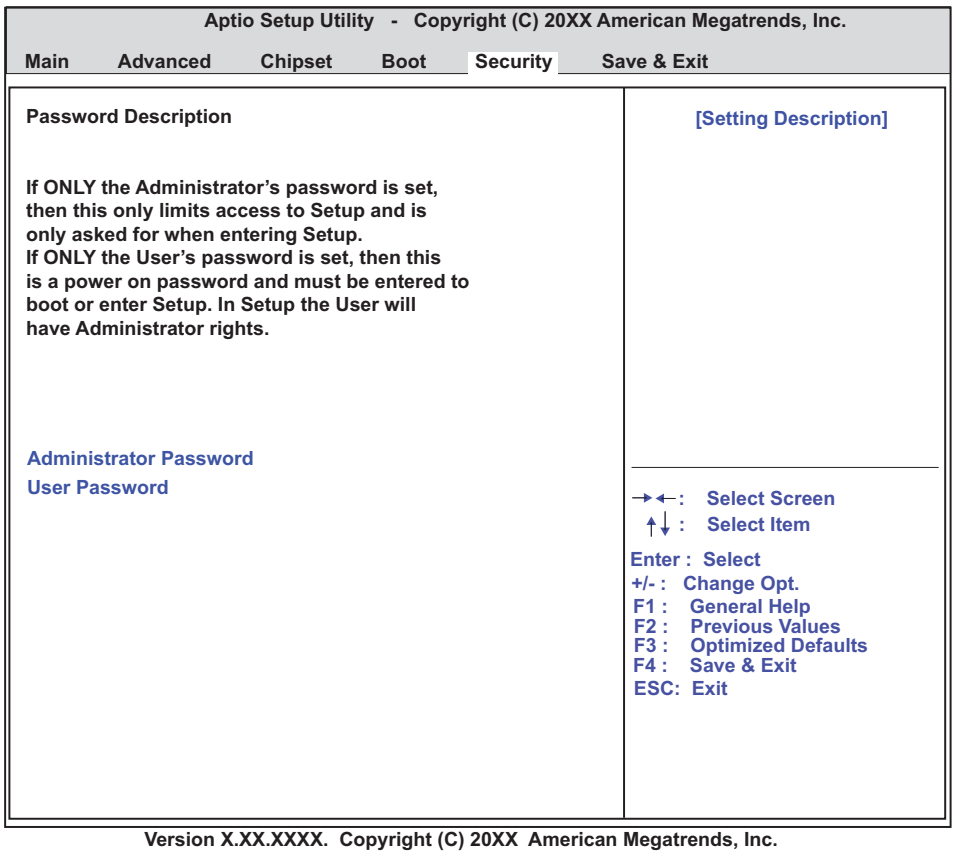
Aptio Setup Utility - Copyright (C) 20XX American Megatrends, Inc.
Main
Advanced
Chipset
Boot
Security
Save & Exit
Password Description
If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup.
If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights.
Administrator Password
User Password
[Setting Description]
→←: Select Screen
↑↓: Select Item
Enter : Select
+/- : Change Opt.
F1 : General Help
F2 : Previous Values
F3 : Optimized Defaults
F4 : Save & Exit
ESC: Exit
Version X.XX.XXXX. Copyright (C) 20XX American Megatrends, Inc.
CM720_BIOS_Security_a

Figure 4-5. Security BIOS Setup Screen

- **Password Description**
  - Administrator Password [Create New Password]
  - User Password [Create New Password]

Save & Exit BIOS Setup Screen

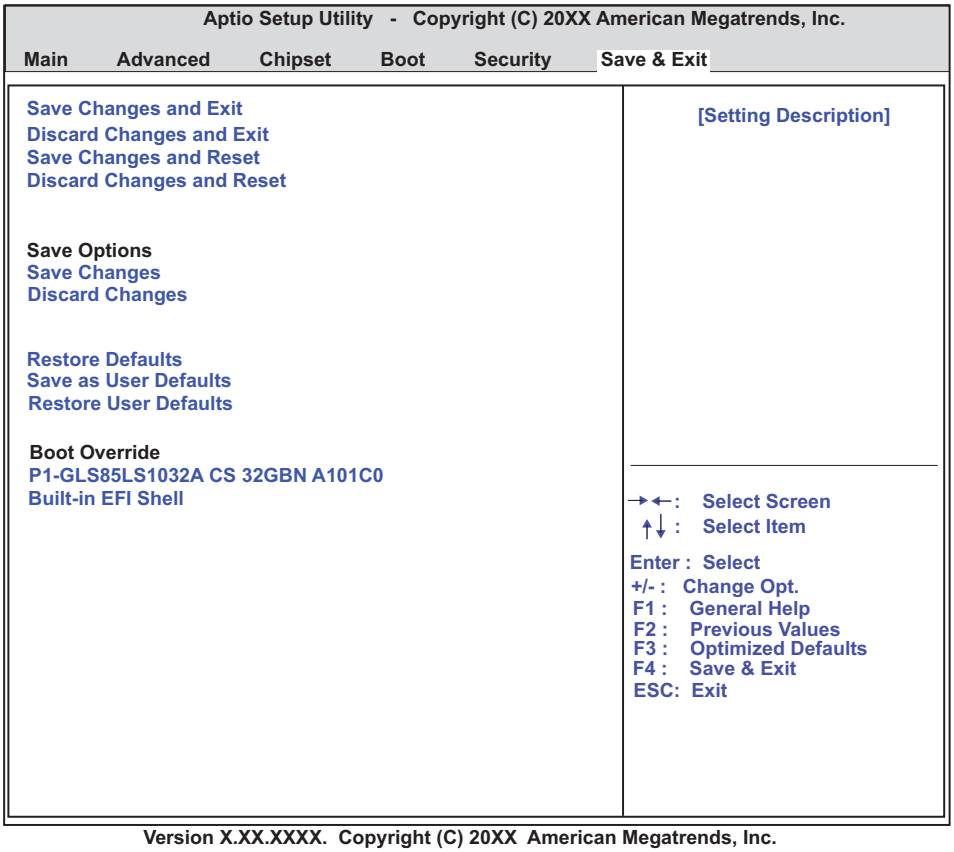

Figure 4-6. Save & Exit BIOS Setup Screen

- **Exit and Reset Options**
  - Save Changes and Exit
    - Save configuration and exit? [**Yes**; No]
  - Discard Changes and Exit
    - Quit without saving? [**Yes**; No] (ESC key can be used for this operation.)
  - Save Changes and Reset
    - Save configuration and reset? [**Yes**; No]
  - Discard Changes and Reset
    - Reset without saving? [**Yes**; No]

- **Save Options**
  - Save Changes
    - Save configuration? [**Yes**; No]
  - Discard Changes
    - Load Previous Values? [**Yes**; No]
  - Restore Defaults
    - Load Optimized Defaults? [**Yes**; No]

- Save as User Defaults
  - Save configuration? [**Yes**; No]
- Restore User Defaults
  - Restore User Defaults? [**Yes**; No]

- **Boot Override**
  - P1-GLS85LS1032A CS 32GBN A101C0
    - Save configuration and reset? [**Yes**; No]
  - Built-in EFI Shell

NOTE	Selecting this setting enters the system into the EFI Shell mode screen.

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed below in Table A-1. Requests for support through the Ask an Expert are given the highest priority, and usually will be addressed within one working day.

- ADLINK's Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro By ADLINK web page at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

  ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called "My ADLINK" unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to My Stuff area where you can check status, update your request, and access other features.

- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1. Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	Contact us should you require any service or assistance. **ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

Table A-1. Technical Support Contact Information (Continued)

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Index

A

AMI BIOS Aptio TSE User's Guide 1
ANSI-compatible serial terminal 34
Atom E6XXT CPU 4, 20

B

Battery
  pin-out list 32
  RTC 33
BIOS Setup Utility
  access 35
  menus 37
  serial console 35
  Splash Screen (OEM Logo) 36
  Watchdog Timer (WDT) 34
block diagram 7
board thickness 14

C

CAN bus interface 31
chip specifications 2
clear CMOS 13
connectors
  header, connector, and socket list 11
  pin sequence 12
console redirection 34
cooling assembly 17
CPU description 5, 20
current capability 29

D

dimensions 14

E

Environmental specifications 16
Ethernet 6, 26
expansion bus specifications 1

F

fan interface 32
features list 5

G

GPIO interface 29

H

headers, connectors, and sockets 11
heatsink requirements 17
Hot cable (modified serial cable) 34

I

I/O address map 22
Interrupt (IRQs) list 21

J

jumper locations 13

L

low voltage limit 29
LVDS voltage 13

M

major integrated circuits 8
mechanical dimensions 15
MiniModules 3

O

Oops! jumper (BIOS recovery) 33

P

PC/104 Architecture 3
pin sequence 12
power
  interface 29
  requirements 16
power interface 29
product description 4

R

Real Time Clock (RTC) 33
references
  CAN specification 1
  I2C specification 1
  LPC specification 1
  PC/104 specification 1
  PCI 3.0 specification 1
  PCIe specification 1
reset switch interface 30

S

serial console 34
  accessing BIOS 35
serial headers 23
site preparation
  environmental considerations 16
SMBus interface 31
speaker interface 30
Splash Screen 36
SSD (Solid State Drive) 33
supported features
  Atom E6XXT CPU 5, 20
  battery 6, 32
  console redirection 34
  DDR2 RAM 5
  Ethernet 6, 26
  external speaker 30
  I/O address map 22
  IRQ assignments 21
  jumper headers 13
  LED, external Ethernet 33
  memory map 21
  Oops! jumper (BIOS recovery) 6, 33
  optional system fan header 32
  PC/104 bus 5
  PC/104-Plus bus 5
  reset switch 30
  SATA interface 5

serial console 6, 34
serial ports 5, 23
SMBus devices 31
Splash Screen (OEM Logo) 36
USB 6, 24
user GPIO signals 29
Utility header 30
video 6
Watchdog Timer 6
System fan interface 32

T

Technical Support 47
thermal cooling
processor requirements 17
thickness 14

U

USB ports 24
Utility header
external speaker connection 30
reset switch connection 30

V

voltage requirements 29

W

Watchdog Timer (WDT) 34
web sites 1
weight 14